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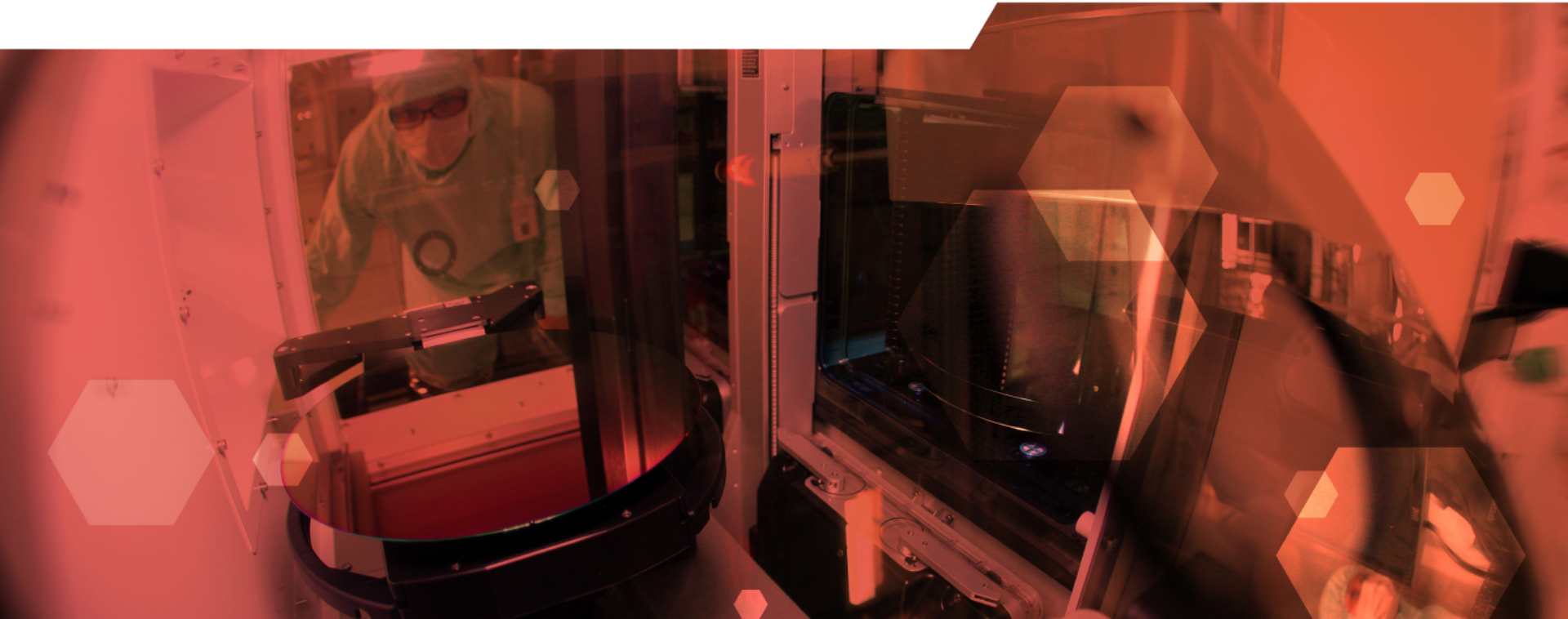
North America Chapter
HB-LED Global Technical Committee

Liaison Report

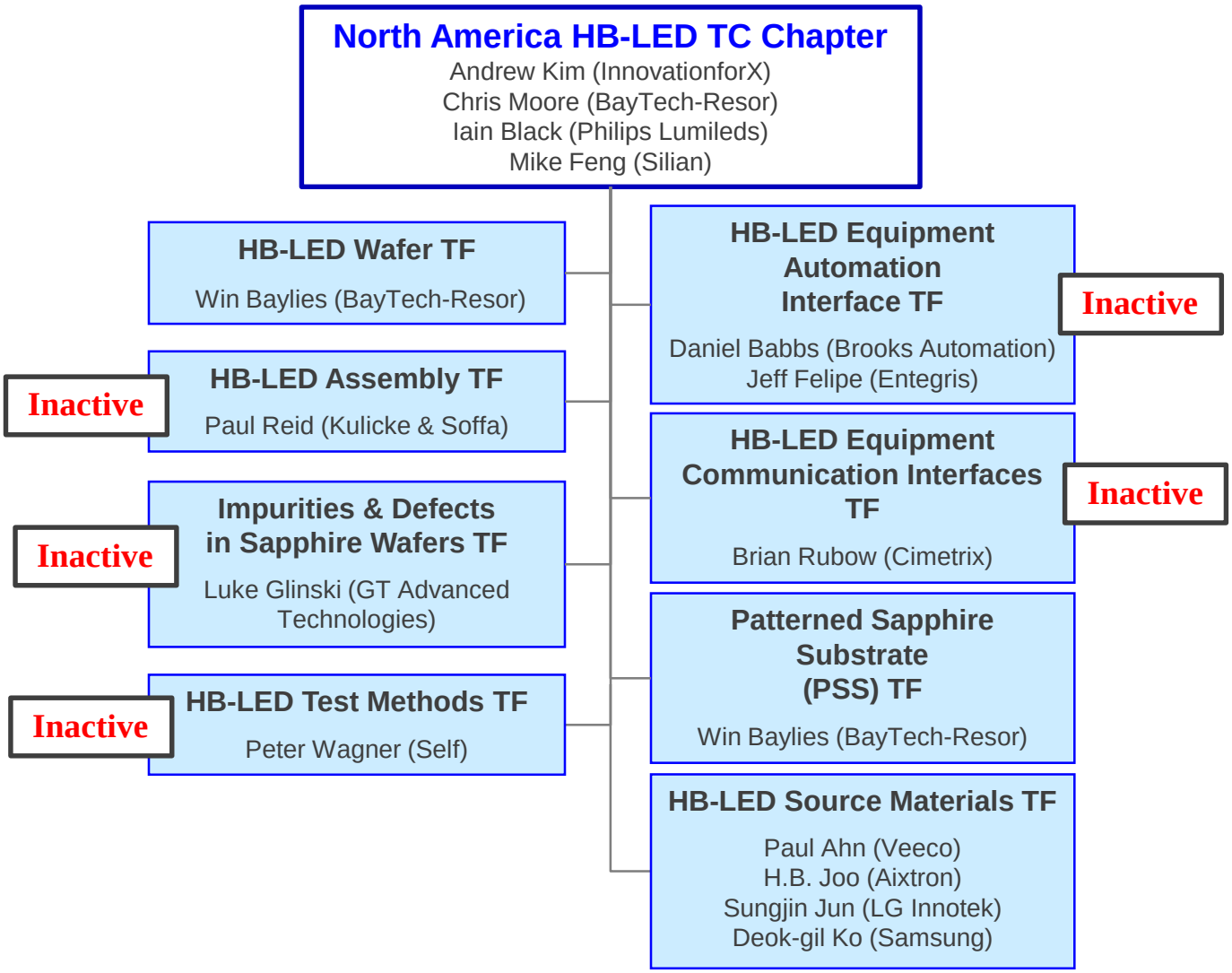
April 2017



Leadership

- NA HB-LED TC Chapter Cochairs
  - Andrew Kim (InnovationforX)
    - New cochair appointed by NARSC at West 2016
  - Chris Moore (BayTech-Resor)
  - Iain Black (Philips Lumileds)
  - Mike Feng (Silian)

HB-LED NA Organization Chart



HB-LED Meeting Information

- Last meetings
  - NA Standards Spring 2017 Meetings on April 6, 2017
    - Location: SEMI Headquarters in Milpitas, CA
- Next meeting
  - SEMICON West 2017 Meetings on July 13, 2016
    - Location: Marriot Marquis in San Francisco, CA

Current Activities

- The NA TC Chapter reviewed a couple of China's documents in the last meeting
  - Doc 5723A and Doc 5775A
  - Comments and feedback sent to Sophia prior to the meetings
- Wafer TF
  - HB-LED Wafer Marking Experiment Project
    - Looking for members to restart this activity
    - Review goals and results and plan for next steps
- HB-LED Patterned Sapphire Substrate (PSS) TF
  - No activity update.
  - Committee may plan to sunset this TF at Fall 2017 Meetings

Next NA HB-LED Standards Meetings
[Tentative]

- SEMICON West 2017 Standards Meetings
  - Location: San Francisco Marriot Marquis Hotel in San Francisco, CA

- Thursday, July 13
  - 09:00 to 10:30
    - Joint HB-LED Wafer/Source Materials/PSS TFs
  - 10:30 to 12:00 Noon
    - NA HB-LED TC Chapter Meeting

Thank you!

For more information or to participate in any NA HB-LED activities, please contact Laura Nguyen (lnguyen@semi.org)

Back Up

Requests [1/2] From Fall Meetings 2015
NA Chapter Request to Regional Counterparts

- Request for participation and general comments
- NA is beginning to describe process defect found in patterned sapphire substrate (PSS)
- The below documents contain preliminary information

- Please provide feedback, comments, and any additional information you think is relevant


PSS(Patterned
hire Substrate) Pro


PSS Defect
Table_V0_2408201

Requests [2/2] From Fall Meetings 2015
NA Chapter Requests to China Chapter

- Define the difference between the two documents:
  - Doc 5723, New Standard: Specification for Single Crystal Sapphire Intended for Use for Manufacturing HB-LED Wafers
  - Doc 5775, New Standard: Specification for Sapphire Single Crystal Ingot Intended for Use for Manufacturing HB-LED Wafers
- Clarify what Doc 5723 applies to, i.e. wafers, ingots/cores, crystals, starting materials
  - Note: single crystal sapphire is too generic of a term
- Please modify existing SNARFs to be more specific in terms of scope and title to include the type of form factor to which it applies, as single crystal sapphire could refer to almost anything
- Scope and title should specify core, ingot, block, wafer, boule, starting material, etc.
- Please make sure that only one standard applies to any particular property/process (there appears to be overlap between Doc 5723 and 5775)

- Double Sided Polished (DSP) Wafers Discussion
  - Reviewed two proposed specifications for 50mm, 100mm and 150mm DSP wafers to be incorporated in SEMI HB1:
    - Proposal 1:
      - Flat Orientation: A-plane (11-20)
      - Flat Length: 32.5 ± 2.5 mm
      - Thickness: 650 ± 25 µm
    - Proposal 2:
      - Diameter: 50, 75, 100.0 ± 0.5 mm
      - Thickness: 300, 400, 650 ± 25µm

- Sapphire Defect Types
  - Currently have photos & brief descriptions of about 10 types
  - The goal is to have an illustrated glossary for Impurities and Defects similar to MF154, Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces
- Current Understanding of Impurities
  - Their effects on sapphire capabilities
  - Inspection and Measurement
- Need
  - More examples & WG members
  - Geographically-separated key interests
  - Industry expertise

Patterned Sapphire Substrates (PSS) Working Group

- PSS elements are produced with different geometries, spacing, and patterns to serve two distinctly different application areas. The WG's initial goal: Develop a Guide for Describing PSS Pattern Elements. John Ciraldo (Rubicon) will develop tables addressing:
- The issues:
  - Informal suggested definitions for "micro-PSS" and "nano-PSS" applications. Typical current values for some of these may be included.
  - A generic process flow with "normal" lithography processing (not including photoresist issues)
  - Publications list
  - Initial defects glossary
- Some basics:
  - µPSS
    - Increases light extraction
  - nano-PSS
    - Improved GaN film (smaller defects)
    - Smaller element heights, too small to fill inter-peak films
    - Higher spatial frequencies