SEMI® INTERNATIONAL STANDARDS

SEMI 3DS-IC Standards Activities

(Three-dimensional Stacked Integrated Circuits)

Liaison Report

September 2015

3DS-IC Standards Committee

Charter

- To explore, evaluate, discuss, and create consensus-based specifications, guidelines, and practices that, through voluntary compliance, will;
  - promote mutual understanding and improved communication between users and suppliers of 3DS-IC materials, carriers, automation systems and devices, and
  - enhance the manufacturing efficiency and capability and shorten time-to-market so as to reduce manufacturing cost in the 3DS-IC industry.

- Committee formed in Fall 2010
- Inaugural meeting held in January 12, 2011

Participating Companies*

AGC Electronics	Entegris	Novati	Sonoscan
Altera	Fujifilm Electronic	Qualcomm	SUMCO
Applied Materials	GLOBALFOUNDRIES	Quartet Mechanics	Suss MicroTec
Brewer Science	iNEMI	ROHM Semiconductor	Tezzaron
Corning	Intel	Rudolph Technologies	Toray Engineering
eda 2 asic	ITRI	SEMATECH	TSMC
Elpida Memory	Neocera	Semilab	Xilinx
	NIST	Shin-Etsu Polymer	

* partial list

Published Standards [1/14]

- SEMI 3D1-0912, *Terminology for Through Silicon via Geometrical Metrology*
  - Clear and commonly accepted definitions are needed for efficient communication and to prevent misunderstanding between buyers and vendors of metrology equipment and manufacturing services.
  - The purpose of this Document is to provide a consistent terminology for the understanding and discussion of metrology issues important to through silicon vias (TSV).

Published Standards [2/14]

- SEMI 3D2-1113, *Specification for Glass Carrier Wafers for 3DS-IC Applications*
  - This Specification describes:
    - dimensional, thermal, and wafer preparation characteristics for glass starting material that will be used as carrier wafers in a temporary bonded state;
    - glass carrier wafers with nominal diameters of 200 and 300 mm, and a thickness of 700 um, although the wafer diameter and thickness required may vary due to process and functional variation. Such variations shall be clarified in the purchasing order or in the contract.
  - Methods of measurements suitable for determining the characteristics in the specifications are indicated.

Published Standards [3/14]

- SEMI 3D3-0613, *Guide for Multi-Wafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames*
  - This Guide is intended to address the needs for choosing a method for shipping thin wafers on tape frames in such a way that they arrive undamaged at their final destination. It describes various methods of shipping thin wafers on tape frames.

Published Standards [4/14]

- SEMI 3D4-0613, *Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks*
  - Control of parameters, such as bonded wafer stack (BWS) thickness, total thickness variation (TTV), bow, warp/sori, and flatness metrology, is essential to successful implementation of a wafer bonding process. These parameters provide meaningful information about the quality of the wafer thinning process (if used), the uniformity of the bonding process, and the amount of deformation induced to the wafer stack by the bonding process.
  - This Guide provides a description of tools that can be used to determine these key parameters before, during, and after the process steps involved in wafer bonding.

Published Standards [5/14]

- SEMI 3D5-0314, *Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures*
  - This Guide aims to assist in the selection and use of tools for performing measurements of geometrical parameters of an individual TSV (through-silicon via), or of an array of TSVs.

Published Standards [6/14]

- SEMI 3D6-0913, *New Standard: Guide for CMP and Micro-bump Processes for Frontside Through Silicon Via (TSV) Integration*
  - This Guide provides:
    - A generic middle-end process flow to define acceptable TSV and CMP quality criteria as well as to develop methodology and measuring procedures for micro-bump.
    - A criteria and common baselines of the middle-end process for related upstream and downstream manufacturers in fabricating 3DS-IC products.

Originated by Taiwan 3DS-IC

Published Standards [7/14]

- SEMI 3D7-0913, *New Standard: Guide for Alignment Mark for 3DS-IC Process*
  - Photo alignment mark configuration is the key to ensure consistent and precise alignment of layers, chips and wafers.
  - This Guide provides:
    - the alignment mark strategy for chip to chip, chip to wafer, and wafer to wafer stacking.
    - addresses the universal alignment mark where the outcome will be a feasible photo alignment standard.

Originated by Taiwan 3DS-IC

Published Standards [8/14]

- SEMI 3D8-0514, *Guide for Describing Silicon Wafers for Use as 300 mm Carrier Wafers in a 3DS-IC Temporary Bond-Debond (TBDB) Process*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure virgin silicon carrier wafers to be used in a 3DS-IC process.

Published Standards [9/14]

- SEMI 3D9-0914, *Guide for Describing Materials Properties for a 300 mm 3DS-IC Wafer Stacks*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure wafer stacks to be used in a 3DS-IC process.

Published Standards [10/14]

- SEMI 3D10-0814, *Guide to Describing Materials Properties for Intermediate Wafers for Use in a 300 mm 3DS-IC Wafer Stack*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure processed wafers to be used in a 3DS-IC process.

Published Standards [11/14]

- SEMI 3D11-1214, *Terminology for Through Glass Via and Blind Via in Glass Geometrical Metrology*
  - This Document provides:
    - clear and commonly accepted definitions of through glass vias (TGV)
    - a consistent terminology for the understanding and discussion of metrology issues important them.
  - This Document focuses on geometry-related metrology and measurands important for definition and control of fabrication and inspection operations on structures that include openings for TGV.

Published Standards [12/14]

- SEMI 3D12-0315, *Guide for Measuring Flatness and Shape of Low Stiffness Wafers*
  - This Guide provides:
    - Definitions for describing a more suitable measurement strategy for low stiffness wafers and geometries.
      - The more suitable measurement process consists of an alternative mounting for wafers with high aspect ratios and the use of high resolution measurements.
    - A measurement procedure for local bow, which denotes small areas of imperfection of the otherwise flat wafer or substrate.
      - This Guide's alternative measurement process is suitable for use in materials acceptance and process control, but may also be useful in other applications, such as wafer design and production.
    - This Document is a guide for a nondestructive procedure that uses a semicontinuous flat mounting surface and high resolution measurement methods.

Published Standards [13/14]

- SEMI 3D13-0715, *Measuring Voids in Bonded Wafer Stacks*
  - This Guide assists users in the selection and use of bond-void metrology equipment and a protocol for performing bond-void measurements based on their application.
    - New bonding processes and applications are sensitive to significantly smaller voids than bonding processes currently used for 3DS-IC package sealing.

- Also published:
  - SEMI AUX032-0715, *Round Robin Study of Method for Measurement of Voids in Bonded Pairs of Silicon Wafers*

Published Standards [14/14]

- SEMI 3D14-0715, *Guide for Incoming/Outgoing Quality control and Testing Flow for 3DS-IC Products*
  - Background: To ensure consistent yield control of 3DS-IC products, common criteria for incoming quality control (IQC) and outgoing quality control (OQC) of outsourced subassembly and test (OSAT) are needed.
  - This Guide defines
    - the criteria for incoming quality control (IQC) and outgoing quality control (OQC) of OSATs, such as appearance, discoloration, missing ball or crack to clarify the manufacturer's responsibilities and to improve product yield.
    - the generic testing flows for different 3DS-IC products, such as chip on chip (CoC), chip on substrate (CoS), chip on wafer (CoW), stacked chip on substrate (SCoS), and wafer on wafer (WoW) to help accelerate the progress of 3DS-IC testing.
  - The generic testing flows for different 3DS-IC products also be defined in this Guide will expedite the progress of 3DS-IC testing.

Published Standards [Packaging Volume]

- SEMI G96-1014, *Test Method for Measurement of Chip (Die) Strength by Mean of Cantilever Bending*
  - Defines a procedure for evaluation of die strength by mean of cantilever bending where 3 point bending is not easy to measure strength in case of wafer thickness less than 50 µm.
  - Applies only for cantilever bending method, and other methods will be defined by separate documents

SEMI® INTERNATIONAL STANDARDS

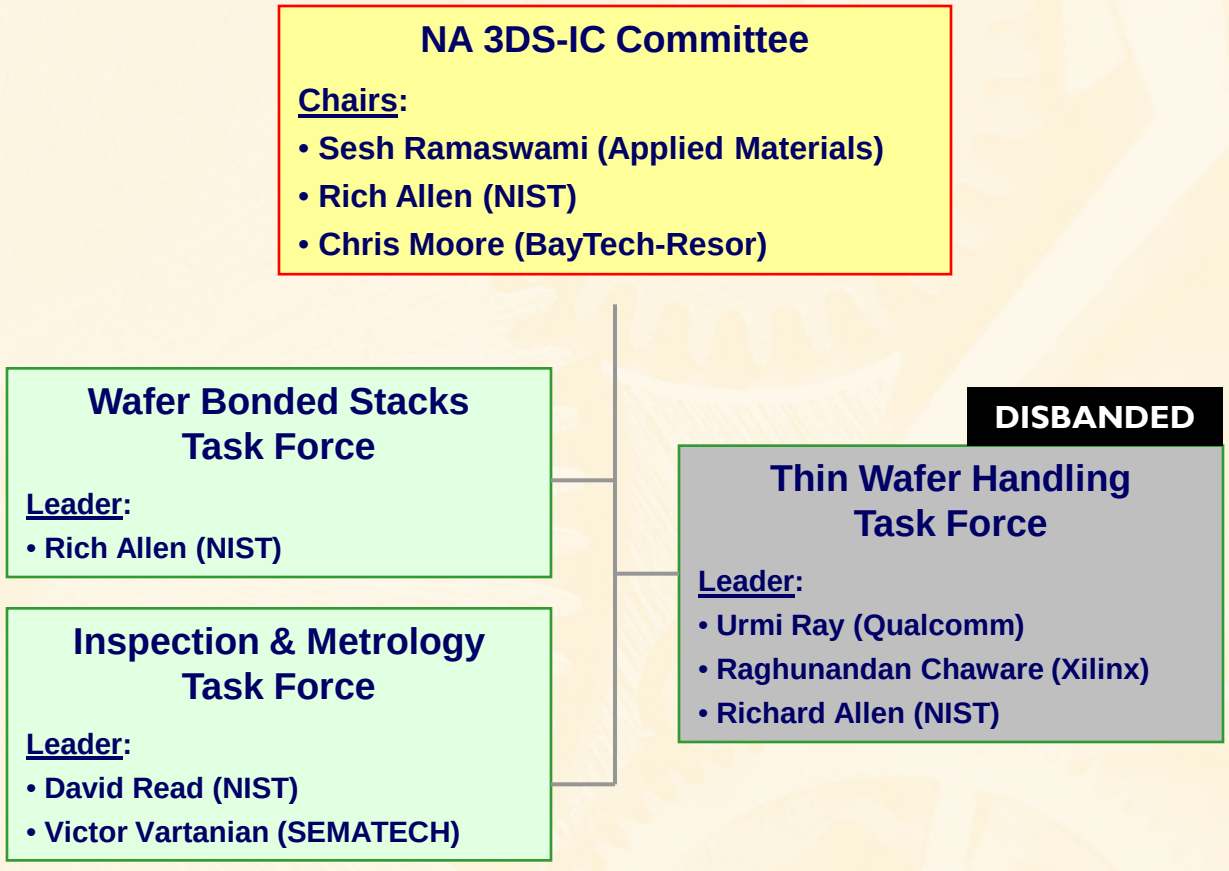
North America 3DS-IC Committee

Overview

Leadership

- Committee Co-chairs
  - Sesh Ramaswami (Applied Materials)
  - Rich Allen (NIST)
  - Chris Moore (BayTech-Resor)

Organization Chart



NA 3DS-IC Task Force Overview

- Bonded Wafer Stacks
  - Create and/or modify specifications that reflect bonded wafer stacks parameters and the wafer bonding process.
- Inspection & Metrology
  - Develop standards for metrology and inspection methods to be used in measuring the properties of TSV's, bonded wafer stacks, and dies used in the 3DS-IC manufacturing process.

Meeting Information

NA 3DS-IC Committee

- Last meeting
  - July 14 for SEMICON West 2015
    San Francisco, California

- Next meeting
  - November 3 for the NA Fall 2015 Meetings
    San Jose, California

Document Review Summary

SEMICON West 2015 Meetings

* Cycle 5, 2015 *		
Doc #	Description	TC Action
5823	Revision to SEMI 3D2-1113, Specification for Glass Carrier Wafers for 3DS-IC Applications	Failed, to be reballoted

Upcoming NA 3DS-IC Ballots

To be reviewed at NA Fall 2015 Meetings

* Voting Period – Cycle 7, 2015 *		
Doc #	Document Title	Task Force
5823A	Revision to SEMI 3D2-1113, Specification for Glass Carrier Wafers for 3DS-IC Applications	Bonded Wafer Stacks TF

SNARFs [1/3]

(Standards New Activity Report Form)

Bonded Wafer Stacks TF	
Doc. 5173	New Standard: Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack
Doc. 5692 *Discontinued*	New Standard: Guide for Describing Glass Wafers for Use as 300 mm Carrier Wafers in a 3DS-IC Temporary Bond-Debond (TBDB) Process
Doc. 5174 *Discontinued*	New Standard: Specification for Identification and Marking for Bonded Wafer Stacks
Doc. 5713 *Revised*	New Standard: Specification for Glass Interposer Base Material without or with Through-Glass or Blind Via Openings (From: New Standard: Specification of Glass Interposers)
Doc. 5823	Revision to SEMI 3D2, Specification for Glass Carrier Wafers for 3DS-IC Applications

SNARFs [2/3]

(Standards New Activity Report Form)

Inspection & Metrology TF	
Doc. 5270 (completed)	New Standard: Guide for Measuring Voids in Bonded Wafer Stacks
Doc. 5447 (completed)	Terminology for Measured Geometrical Parameters of Through-Glass Vias (TGVs) in 3DS-IC Structures
Doc. 5506 (completed)	New Standard: Guide for Measuring Flatness and Shape of Low Stiffness Wafers
Doc. 5616 (completed)	Revision to SEMI 3D4, Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

SNARFs [3/3]

(Standards New Activity Report Form)

Inspection & Metrology TF *(cont'd)*	
Doc. 5766 (completed)	New Auxiliary Information: Round Robin Study of Method for Measurement of Voids in Bonded Pairs of Silicon Wafers – Supporting SEMI Draft Document 5270, Guide for Measuring Voids in Bonded Wafer Stacks
Doc. 5822	New Standard: Specification for Reference Material for Bonded Wafer Stack Void Metrology

Current Activities [1/4]

- [#5173] *New Standard: Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack*
  - Bonded Wafer Stack TF
  - Rationale
    - Current wafer standards (SEMI M1) do not adequately address the needs of wafers used in bonded wafer stacks.
  - Scope
    - This Guide:
      - provides the tools to acquire silicon wafers that will be used in 3DS-IC applications as device wafers.
      - describes silicon wafers with nominal diameter of 300 mm although, for 3DS-IC applications, the actual wafer diameter may differ slightly due to process requirements.

Current Activities [2/4]

- [#5823] Revision to SEMI 3D2, *Specification for Glass Carrier Wafers for 3DS-IC Applications*
  - Bonded Wafer Stacks TF
  - Background
    - SEMI 3D2-1113 was originally developed to provide the framework for ordering Glass Wafers for the application of carrier wafer for processing device wafers for 3D stacking.
    - As this technology has matured, the requirements for such carrier wafers have become more clear and weaknesses in 3D2-1113 have been identified.
    - This activity aims to revise SEMI 3D2-1113 to address the following weaknesses:
      - Update or eliminate specifications that are unnecessarily stringent for 3D stacked applications
      - Allow for additional glass types that were not permitted in 3D2-1113, yet meet industry requirements for 3D stacked applications.
    - This Document development activity is expected to result in a major revision of 3D2.

Current Activities [3/4]

- [#5713] *New Standard: Specification for Glass Interposer Base Material without or with Through-Glass or Blind Via Openings*

  (Title revised, formerly: *New Standard: Specification of Glass Interposers)*

  - Bonded Wafer Stack TF
  - Background: In the past, interposers were made from silicon. Glass can be used as an alternative material with its specific physical and thermal properties. However, no specification or description of requirements for such glass interposers exists.
  - This document will include specifications for procuring glass base material intended for use as an interposer. The glass base material may be in the form of a wafer or a panel.
    - This specification describes dimensional and thermal characteristics of glass with openings and glass for interposers.
    - Methods of measurements suitable for determining the characteristics in the specification are indicated.
  - This document will also include specifications for procuring glass base material with TGV or Blind Via openings.

Current Activities [4/4]

- [#5822] New Standard: *Specification for Reference Material for Bonded Wafer Stack Void Metrology*
  - Inspection & Metrology TF
  - Rationale
    - The Guide for Measuring Voids in Bonded Wafer Stacks (SEMI Draft Document 5270) is soon to be published as a 3DS-IC Standard. Document 5270 summarizes the state of the art in 2013/2014 for void detection. Going forward, a test sample of known void dimensions will be needed for metrology system development and calibration. This SNARF describes a document which will be used to create such a sample.
  - Scope
    - Describe requisite test structures, including design, manufacturing, and certification procedure.

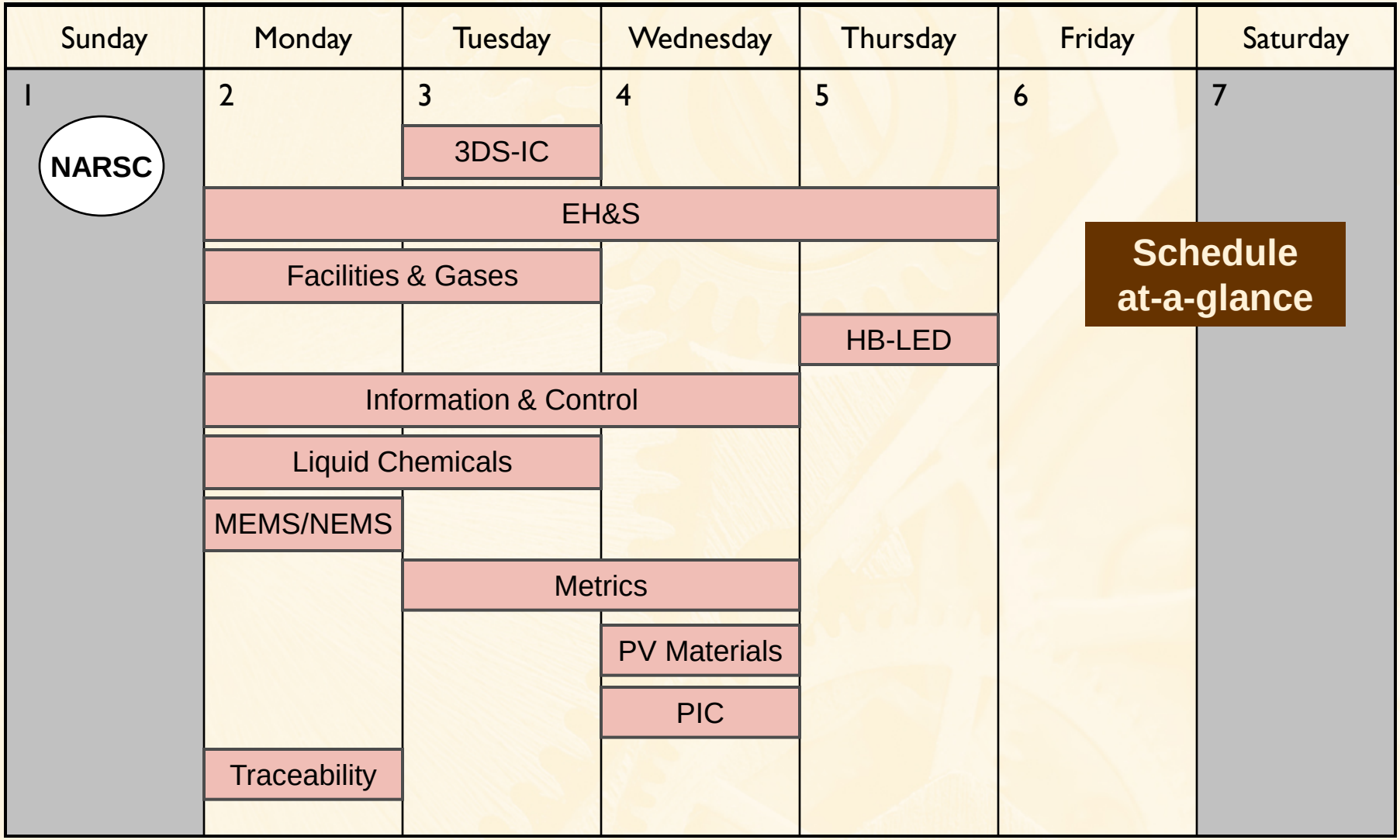
NA 3DS-IC Meeting Schedule

- NA Standards Fall 2015 Meetings
  - November 2-5, 2015
  - SEMI Headquarters
  - 3081 Zanker Road
  - San Jose, California 94103
  - U.S.A.

  - Tuesday, November 3
    - Inspection & Metrology TF (9:00 AM to 10:30 AM)
    - Bonded Wafer Stacks TF (10:30 AM to 12:00 Noon)
    - NA 3DS-IC Committee (1:30 PM to 3:30 PM)

NA Standards Fall 2015 Meetings

November 1-5



Thank you!

- For more information, please visit the SEMI 3DS-IC Google Site:
  - https://sites.google.com/a/semi.org/3dsic/

- For more information or to participate in any NA 3DS-IC activities, please contact:
  - Kevin Nguyen
    SEMI North America Standards
    knguyen@semi.org