SEMI China Compound Semiconductor Materials Std. Technical Committee

4H-SiC Epitaxial Wafer Task Force

Gan Feng

General Manager

Epiworld International Co., LTD

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Leaders of 4H-SiC Epitaxial Wafer Task Force

No.	Name	Company	Industry Chain
1	Gan Feng 冯淦	Epiworld International Co., LTD 瀚天天成电子科技（厦门）有限公司	Epitaxial 外延生产企业

Vice leaders of 4H-SiC Epitaxial Wafer Task Force

No.	Name	Company	Industry Chain
1	Guosheng Sun 孙国胜	Institute of Semiconductors, CAS 中科院半导体所	Epitaxial Research Institute 外延研究机构

Members of 4H-SiC Epitaxial Wafer Task Force

No.	Name	Company	Industry Chain
1	Zhixia chen 陈志霞	Epiworld International Co., LTD 瀚天天成电子科技（厦门）有限公司（外延）	Epitaxial 外延生产企业
2	Yi Wang 王翼	The 55th Research Institute of China Electronics Technology Group Corporation 中国电子科技集团第五十五研究所	Epitaxial 外延生产企业
3	Weili lu 芦伟立	Heibei Semiconductor Research Institute 中国电子科技集团第十三研究所	Epitaxial 外延生产企业
4	Chengzhan Li 李诚瞻	CRRC Times Semiconductor Co., LTD 株洲中车时代电气股份有限公司	Device 器件制作企业
5	Jianxin Ji 计建新	TOPE Technologies Co.,LTD 绍兴澎芯半导体有限公司	Device 器件制作企业
6	Guanagyan Shi 施广彦	Global Power Technology Co., LTD 泰科天润半导体科技（北京）有限公司	Device 器件制作企业
7	Yingmin Wang 王英民	Shanxi Semicore Crystal Co., LTD 中国电子科技集团第二研究所	Substrate 衬底生产企业
8	Zongjing She 佘宗静	Tankeblue Semiconductor Co., Ltd 北京天科合达半导体股份有限公司	Substrate 衬底生产企业
9	Tom Barbieri	Wolfspeed	Substrate & Epitaxial 衬底 & 外延生产企业

New members of 4H-SiC Epitaxial Wafer Task Force

No.	Name	Company	Industry Chain
1	倪炜江	安徽芯塔电子科技有限公司	Device 器件制作企业
2	赵丽丽	哈尔滨科友半导体产业装备与技术研究院有限公司	Scientific Research Institute 科研院所

Documents in Work

SEMI Draft Document： 4H-SiC Homoepitaxial Wafer Specification 4H-SiC同质外延片标准

➢ 1、Timetable for Document Completion 标准计划完成时间

No.	Milestones	Completion date
1	Date Prepared	Aug-20
2	Activity start	Nov-20
3	1st Draft	Oct-21
4	Letter Ballot	Jun-22
5	TC Chapter Approval	Dec-22

Documents in Work

SEMI Draft Document： 4H-SiC Homoepitaxial Wafer Specification 4H-SiC同质外延片标准

➢ 2、Progress of Documents Work 标准工作进展

The first draft of the standard has been completed in early Sep. 2021，and apply for global voting in Jan. 2022 . 标准的初稿已于2021年9月初完成，并申请于2022年1月进行全球投票。

本标准适用于在n型4H-SiC衬底上生长的n型4H-SiC外延片，主要规定了以下十个部分内容：This standard is applicable to 4H-SiC homo-epitaxial wafers grown on n-type 4H-SiC substrates. It mainly stipulates the following seven parts：

- ➢1、目的 Purpose
- ➢2、范围 Scope
- ➢3、规范性引用文件 Referenced Standards and Documents
- ➢4、术语和定义 Terminology
- ➢5、订单信息（Ordering Infromation)
- ➢6、技术要求 Requirements
- ➢7、检验方法 Test Methods
- ➢8、检验规则 Sampling
- ➢9、合格证书 Certification
- ➢10、包装和标志 Packaging and Marking

SEMI Draft Document 6693
New Standard: 4H-SIC HOMOEPITAXIAL WAFER SPECIFICATION

1 Purpose

1.1 The specification covers the requirements for 4H-SiC homoepitaxial wafers used in power device manufacturing.

1.2 The specification provides a uniform standard of 4H-SiC homoepitaxial wafers for the suppliers and the customers in the industrial chain.

2 Scope

2.1 The specification specifies the parameters of 4H-SiC homoepitaxial wafers whose epitaxial layer is grown on an n-type substrate.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Polished Wafers

SEMI M55 — Specification for Polished Monocrystalline Silicon Carbide Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M81 — Guide to Defects Found on Monocrystalline Silicon Carbide Substrates

SEMI M83 — Test Method for Determination of Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors

SEMI M154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gauge

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1392 —Test Method for Determining Net Carrier Density Profiles in Silicon Wafers By Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafer by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T5 — Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers

3.2 ASTM Standard

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

3.3 ASQ Standard

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, SEMI M55 and SEMI M59.

4.1 Abbreviations and Acronyms

4.1.1 *AFM* — atomic force microscope, an instrument for measuring microroughness.

4.1.2 *C-V* — capacitance - voltage method for measuring carrier concentration of epitaxial layer.

4.1.3 *FT-IR* — fourier transform infrared (spectrometer), a method for measuring the thickness of epitaxial layer.

4.1.4 *GBIR* — flatness property.

4.1.4.1 Discussion — See SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as 'local indicator reading (TTV)'.

4.1.5 *SBIR* — flatness property.

4.1.5.1 Discussion — See SEMI M1, Appendix 1, Flatness Decision Tree. Formerly also known as 'local thickness variation (LTV or LTVmax)'.

4.2 Definitions

4.2.1 *area contamination* — any foreign matter on the surface in localized areas that is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains or water spots, etc.

4.2.2 *basal plane dislocation (BPD)* — dislocation lying on the basal plane.

4.2.3 *buffer layer* — a transition layer epitaxially-formed between a substrate and the first epitaxial layer.

4.2.4 *carrot defect* — a carrot-shaped defect on the epitaxial layer surface, which is consisting a basal plane stacking fault terminating at a Frank partial dislocation and a prismatic fault terminating at the epitaxial layer surface.

4.2.5 *crack* — cleavage or fracture that extends to the surface of a wafer.

4.2.6 *dislocation* — a line imperfection in a crystal lattice that is characterized by a closure failure of Burgers' circuit that may form the boundary between slipped and non-slipped areas of a crystal or occur at the edge of stacking faults or around precipitates such as oxide precipitates.

4.2.7 *downfall* — a macroscopic size particle existing within or extending beyond the epitaxial layer. The crystal structure of the particles is usually 3C.

4.2.8 *edge chip* — region where material has been unintentionally removed from the edge of the wafer.

4.2.9 *edge exclusion (EE)* — the distance from the FQA boundary to periphery of a wafer of nominal dimensions. See definition of fixed quality area below.

4.2.10 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion, EE over which the specified values of a parameter apply. Because the nominal edge exclusion relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances.

4.2.11 *homoepitaxial layer* — thin monocrystalline film epitaxially-formed on a substrate of the same material and crystallographic orientation, inheriting the atomic order of the substrate.

4.2.12 *micropipe (MP)* — small hollow tube basically parallel to the crystallographic c-axis and extending typically through larger parts of the crystal boule and thus affecting several neighboring wafers. Micropipes may be generated at bulk defects e.g. inclusions, polytype defects or crystallites. (See SEMI M81 for examples.)

4.2.13 *polytype* — one of the modifications of monocrystalline material which shows polytypism.

4.2.14 *polytypism* — phenomenon where a material occurs in several structural modifications, each of which can be regarded as built up by stacking layers of identical structure and chemical composition.

4.2.15 *scratch* — a shallow groove or cut below the established plane of the surface of a semiconductor wafer, with a length to width ratio greater than 5:1.

4.2.16 *silicon carbide (SiC)* — semiconductor crystal composed of silicon and carbon, which will exhibits a large number of polytypes such as 3C-, 4H-, 6H-, and 15R-.

Note: A symbol like 4H- gives the number of periodic stacking bilayers (2, 3, 4.....) and the crystal symmetry (H=hexagonal, C=cubic, and R= Rhombohedral) of each polytype.

4.2.17 *substrate* — a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits that may be fabricated directly in the substrate or in a film of the same or another material grown or deposited on the substrate.

4.2.18 *surface killer defect* — surface killer defects are including downfall, triangular defect and carrot defect.

4.2.19 *threading edge dislocation (TED)* — edge dislocation penetrating through the crystal approximately normal to the basal plane.

4.2.20 *threading screw dislocation (TSD)* — screw dislocation penetrating through the crystal approximately normal to the basal plane.

4.2.21 *total usable area* — the proportion of the area of the wafer without surface killer defects to the area of the entire wafer.

4.2.22 *triangular defect* — a triangle-shaped defect on the epitaxial layer surface, which is a lamellar inclusion with a cubic (3C) stacking sequence, so-called "3C inclusion", extending toward the epitaxial layer surface.

(The following show proper formatting of sections. Sections shown are not required, unless otherwise indicated as mandatory.)

5 Ordering Information

5.1 Purchase orders for 4H-SiC epitaxial wafers furnished to this specification shall include the following items from substrate, buffer layer and epitaxial layer. In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

5.2 Substrate

5.2.1 Crystal Polytype

5.2.2 Conductivity Type

5.2.3 Dopant

5.2.4 Resistivity

5.2.5 Wafer Surface Orientation

5.2.6 Diameter

5.2.7 Thickness

5.2.8 Primary Flat Orientation

5.2.9 Primary Flat Length

5.2.10 Secondary Flat Orientation (or none)

5.2.11 Secondary Flat Length (or none)

5.2.12 Substrate Vendor

5.2.13 MP density

5.2.14 TSD density

5.2.15 TED density

5.2.16 BPD density

5.2.17 GBIR

5.2.18 SBIR

5.2.19 Warp

5.2.20 Bow

5.3 Buffer layer

5.3.1 The conductivity type and dopant of buffer layer

5.3.2 The thickness and carrier concentration of buffer layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer.

5.4 Epitaxial Layer

5.4.1 Conductivity type and dopant of each layer

5.4.2 Thickness of each epitaxial layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer (Tolerance / Intra-wafer Uniformity / Test Pattern / Test Method / Edge Exclusion)

5.4.3 Carrier concentration of each epitaxial layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer (Tolerance / Intra-wafer Uniformity / Test Pattern / Test Method / Edge Exclusion)

5.4.4 Surface killer defect and a description of the test method used to measure it (Total usable area / Edge Exclusion)

5.4.5 Surface roughness, and a description of the test method used to measure it

5.4.6 Surface scratch

5.4.7 Edge Chip

5.4.8 Crack

5.4.9 Area contamination (Surface / Backside)

5.4.10 GBIR

5.4.11 SBIR

5.4.12 Warp

5.4.13 Bow

6 Requirements

6.1 The specified parameters of epitaxial wafer shall conform to the requirements of § 6.2 & § 6.3 & § 6.4, otherwise agreed to between the supplier and the customer.

6.2 Substrate

6.2.1 Polytype: 4H

6.2.2 Conductivity type: n-type

6.2.3 Dopant: Nitrogen

6.2.4 Surface orientation: (0001) face 4.0° toward ⟨11$\bar{2}$0⟩

6.2.5 Other specific technical parameters of substrates must meet the requirements of SEMI M55, or must meet the requirements of the specification agreed by the supplier and the customer.

6.3 Buffer layer

6.3.1 Conduction type: n-type

6.3.2 Dopant: Nitrogen

6.3.3 Thickness and carrier concentration

6.3.3.1 The thickness and carrier concentration of buffer layer should meet the requirements of Table 1.

Table 1. The specification of buffer layer

Parameter	*Value (Deviation from Target)*	*Test Condition / Technique*
Thickness, center point	0.5 ~ 1.0 μm (±0.25 μm)	Determine by a method agreed upon between the supplier and the customer.
Carrier Concentration, center point	IE18 cm^{-3} (±50 %)	

6.4 Epitaxial layer

6.4.1 Conduction type: n-type / p-type

6.4.2 Dopant: Nitrogen / Aluminum

6.4.3 Carrier concentration

6.4.3.1 Test pattern

6.4.3.1.1 The test pattern of carrier concentration of epitaxial layer is shown in Figure 1.

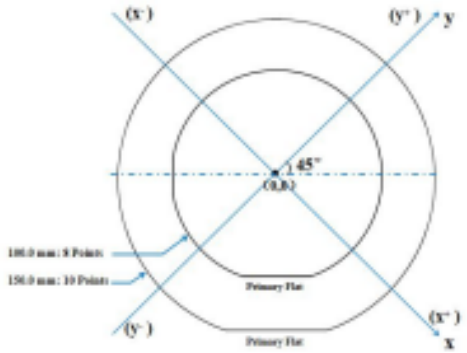

Figure 1. Test Pattern of Carrier Concentration

6.4.3.2 Coordinate of test points

6.4.3.2.1 The coordinate of each test point should meet the requirements of Table 2.

Table 2. Coordinate of Test Points

Test point (mm) / *Wafer diameter*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*
100.0 mm	(-45,0)	(-30,0)	(-20,0)	(-10,0)	(0,0)	(0,45)	(45,0)	(0,-45)		
150.0 mm	(-70,0)	(-65,0)	(-52,0)	(-39,0)	(-26,0)	(-13,0)	(0,0)	(0,52)	(52,0)	(0,-52)

6.4.3.3 Calculation method

6.4.3.3.1 Average of carrier concentration: average value of each test point, and the calculation formula is shown as follows:

$$\overline{N} = \frac{\sum_{i=1}^{n} N_i}{n} \quad (1)$$

where:

N_i = concentration value of the i-th test point, unit: cm^{-3}.

n = number of all test points, the number of test points for wafers with diameters of 100.0 mm and 150.0 mm is 8 and 10, respectively.

$\overline{N}$ = average of carrier concentration, unit: cm^{-3}.

6.4.3.3.2 Tolerance of carrier concentration: The deviation between average and target of carrier concentration, and the calculation formula is shown as follows:

$$\text{Tolerance} = \frac{\overline{N}-\text{Target}}{\text{Target}} \times 100\% \quad (2)$$

where:

$\overline{N}$ = average of carrier concentration, unit: cm^{-3}.

Target = target of carrier concentration for epitaxial growth.

6.4.3.3.3 Uniformity of carrier concentration: the calculation formula is shown as follows:

$$\text{Uniformity} = \frac{\sigma}{\overline{N}} \times 100\% \quad (3)$$

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n} (N_i-\overline{N})^2}{n}} \quad (4)$$

where:

Uniformity = uniformity of carrier concentration.

σ = Standard deviation between carrier concentration values at all test points.

$\overline{N}$ = average of carrier concentration, unit: cm^{-3}.

N_i = concentration value of the i-th test point, unit: cm^{-3}.

n = number of all test points, the number of test points for wafers with diameters of 100.0 mm and 150.0 mm is 8 and 10, respectively.

6.4.3.4 The specification of carrier concentration should meet the requirements of Table 3.

Table 3. The specification of Carrier Concentration

Parameter	*Specification*			*Test Condition / Technique*
Carrier	Average (cm^{-3})	Tolerance (%)	Uniformity (%)	

Concentration	9E14 ~ 5E17	±15	<10	C-V measurement / SEMI MF1392

6.4.4 Thickness

6.4.4.1 The test pattern, coordinate of test points and calculation method of thickness are consistent with the test of carrier concentration, referring to § 6.4.3.1 & § 6.4.3.2 & § 6.4.3.3.

6.4.4.2 The specification of thickness should meet the requirements of Table 4.

Table 4. The specification of Thickness

Parameter	*Specification*			*Test Condition / Technique*
Thickness	Average (μm)	Tolerance (%)	Uniformity (%)	
	2 ~ 30	±10	<10	FT-IR measurement / SEMI MF95

6.4.5 Surface defect

6.4.5.1 Surface killer defect

6.4.5.1.1 The surface killer defect of epitaxial layer should meet the requirements of Table 5.

Table 5. The specification of surface killer defect

Parameter	*Specification*	*Test Condition / Technique*	*Note*
Total usable area (%)	≥95	Determine by a method agreed upon between the supplier and the customer.	#1

#1: The parameter of total usable area is defined in § 4.2.21, and it is calculated by 2 mm x 2 mm grid size. The measurement area is the entire wafer surface except for 3 mm edge exclusion area.

6.4.5.2 Surface scratch

6.4.5.2.1 The surface scratch of epitaxial layer should meet the requirements of Table 6.

Table 6. The specification of surface scratch

Parameter	*Specification*	*Test Condition / Technique*	*Note*
Surface scratch	cumulative length <1x wafer diameter	high intensity light, unaided eye / SEMI MF523	#1

#1: The measurement of areas is the entire wafer surface.

6.4.6 Surface roughness

6.4.6.1 The surface roughness of epitaxial layer should meet the requirements of Table 7.

Table 7. The specification of surface roughness

Parameter	*Specification*	*Test Condition / Technique*
Surface roughness, center 10 μm x 10 μm area	< 0.5 nm	AFM measurement / SEMI M40

6.4.7 Edge chip

6.4.7.1 The edge chip of epitaxial layer should meet the requirements of Table 8.

Table 8. The specification of edge chip

Parameter	*Specification*	*Test Condition / Technique*	*Note*
Edge chip	None with length ≥1.5 mm or depth ≥1.0 mm.	high intensity light, unaided eye / SEMI MF523	#1

#1: Chips measuring < 0.5mm in either length or depth are excluded from this definition. The measurement of areas is the entire wafer surface.

6.4.8 Crack

6.4.8.1 The crack of epitaxial layer should meet the requirements of Table 9.

Table 9. The specification of crack

Parameter	*Specification*	*Test Condition / Technique*
Crack	None	high intensity light, unaided eye / SEMI MF523

6.4.9 Area contamination

6.4.9.1 The area contamination of epitaxial layer should meet the requirements of Table 10.

Table 10. The specification of Area contamination

Parameter	*Specification*	*Test Condition / Technique*
Area contamination	None	high intensity light, unaided eye, the entire wafer surface / SEMI MF523

6.4.10 Flatness

6.4.10.1 The flatness of epitaxial layer should meet the requirements of Table 11.

Table 11. The specification of flatness

Parameter	*Specification*	*Test Condition / Technique*
GBIR (μm)	≤ 10	SEMI MF1530
SBIR (μm)	≤ 5	SEMI MF1530
Warp (μm)	≤ 50	SEMI MF1390
Bow (μm)	≤ 30	SEMI MF1390

7 Test Methods

7.1 Measurements shall be carried out according to the methods outlined in Table 12. Where no methods are specified, or where choices are given, the supplier and the customer shall agree in advance.

7.2 Given the lack of standard reference materials, it is advisable that the supplier and the customer exchange samples to cross calibrate their measurement instruments and procedures.

Table 12. Parameter and Recommended Test Method

Category	*Parameter*	*Test Method*
Substrate	Polytype	None as yet
	Conductivity Type (Dopant)	None as yet
	Resistivity	SEMI MF673
	Surface Orientation	SEMI MF26
	Diameter	SEMI MF2074
	Thickness	SEMI MF533 or SEMI MF1530
	Primary Flat Orientation	SEMI MF847
	Primary Flat Length	SEMI MF671
	Secondary Flat Orientation	SEMI MF847
	Secondary Flat Length	SEMI MF671
	MP Density	None as yet
	TSD density	KOH etched surface, SEMI M83 or ASTM F1404
	TED density	KOH etched surface, SEMI M83 or ASTM F1404
	BPD density	KOH etched surface, SEMI M83 or ASTM F1404
	GBIR	SEMI MF1530
	SBIR	SEMI MF1530
	Warp	SEMI MF1390
	Bow	SEMI MF1390
Buffer layer	Polytype	None as yet

	Conductivity Type (Dopant)	None as yet
	Carrier Concentration	None as yet
	Thickness	None as yet
Epitaxial layer	Polytype	None as yet
	Conductivity Type (Dopant)	None as yet
	Carrier Concentration	SEMI MF1392
	Thickness	SEMI MF95
	Surface killer defect	Determine by a method agreed upon between the supplier and the customer
	Surface scratch	SEMI MF523
	Surface roughness	SEMI M40
	Edge chip	SEMI MF523
	Crack	SEMI MF523
	Area contamination	SEMI MF523
	GBIR	SEMI MF1530
	SBIR	SEMI MF1530
	Warp	SEMI MF1390
	Bow	SEMI MF1390

8 Sampling

8.1 Unless otherwise specified, ASTM E122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the customer.

9 Certification

9.1 Upon request of the customer in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 The customer and supplier may agree that the material shall be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in § 6 to § 7, however, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Labeling

10.1 Special packing and marking requirements shall be subject to agreement between the supplier and the customer. Otherwise, all the wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination in accordance with the best industry practices to provide sample protection against damage during shipment.

10.2 The wafers shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductive dopant (structure), quantity, and lot number.