3DS-IC North America TC Chapter

Meeting Summary and Minutes

SEMICON West 2016 Meetings

Tuesday, July 12, 2016, 13:30 – 15:30

SF Marriott Marquis in San Francisco, California

TC Chapter Announcements

Next TC Chapter Meeting

NA Standards Fall 2016 Meetings

Tuesday, November 8, 2016, 13:30 – 15:30

SEMI Headquarters in San Jose, California

Table 1 Meeting Attendees

Italics indicate virtual participants

Co-Chairs: Sesh Ramaswami (Applied Materials), Richard Allen (NIST), Chris Moore (BayTech-Resor)
SEMI Staff: Laura Nguyen, Chie Yanagisawa

Company	*Last*	*First*	*Company*	*Last*	*First*
Asahi Glass	Takahashi	Mark	Self	Wagner	Peter
BW & Associates	Wu	Bevan	Silicon Solar	Perroots	Len
Corning	Schmidt	Ilona	Sonoscan	Martell	Steve
Evergreen Enhancement	*Kerr*	*Bill*	SuperSight	Perroots	Len
Formfactor	Loranger	Marc			
IPC	Solberg	Vern	SEMI Japan	Yanagisawa	Chie
NIST	Allen	Richard	SEMI	Nguyen	Laura

Table 2 Leadership Changes

Group	*Previous Leader*	*New Leader*
None.		

Table 3 Ballot Results

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

Document #	*Document Title*	*Committee Action*
5713A	New Standard: Specification For Glass Base Material For Semiconductor Packaging	**Passed,** superclean

Table 4 Authorized Activities

#	*Type*	*SC/TF/WG*	*Details*
6075	SNARF	Bonded Wafer Stacks TF	New Standard: Guide for Describing Glass-Based Material for Use in 3DS-IC Process – SNARF to complete the two-week member review and approval by GCS after West

Table 4 Authorized Activities

#	Type	SC/TF/WG	Details
6076	SNARF	Bonded Wafer Stacks TF	New Standard: Specification for Identification and Marking for Bonded Wafer Stacks – SNARF to complete the two-week member review and approval by GCS after West

NOTE 1: SNARFs and TFOFs are available for review on the SEMI Web site at: http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 5 Authorized Ballots

#	When	SC/TF/WG	Details
None.			

Table 6 New Action Items

Item #	Assigned to	Details
2016July#01	Len & Bill	To summarize survey results and send out to the members.
2016July#02	Laura Nguyen	Send email of winner of survey results.

Table 7 Previous Meeting Action Items

Item #	Assigned to	Details
None.		

1 Welcome, Reminders, and Introductions

Richard Allen called the meeting to order at 13:35. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

Attachment: SEMI Standards Required Meeting Elements

2 Review of Previous Meeting Minutes

The TC Chapter reviewed the minutes of the previous meeting.

Motion: To accept the previous meeting minutes as written with edits.
By / 2nd: Steve Martell (Sonoscan) / Ilona Schmidt (Corning)
Discussion: None.
Vote: 6-0 in favor. Motion passed.

Attachment: [2016Spring] NA 3DS-IC Minutes FINAL edits 20160712

3 Liaison Reports

3.1 *Japan TC Chapter*

Laura Nguyen (SEMI) reported for the 3DS-IC Japan TC Chapter. The key items were as follows:

- Outline
- Committee Cochairs: Masahiro Tsuriya (iNEMI), Haruo Shimamoto (AIST)
- Organization Chart *{See attachment for Figure}*
- Meeting Information
  - Last meeting – Japan Spring 2016 Meetings: Friday, April 15, 2016 at SEMI Japan office, Tokyo

  - Next meeting – Japan Spring 2016 Meetings: Tuesday, September 6, 2016 at SEMI Japan office, Tokyo
- TF / SG Updates
  - Steering Group
    - Approved at Kick-off meeting of 3DS-IC Japan TC Chapter held on Sept. 7, 2015
      - Leadership: Yoshihiro Tomita / Intel, Masahiro Tsuriya/ iNEMI, Eiji Yoshino / Hitachi High-Technologies was newly appointed.
    - Charter
      - Define the work areas and review the global TC charter
      - Provide the following inputs and opportunities;
        - Plan technical workshop to promote the latest technologies and market trends on the 3DIC/SiP.
        - Brainstorm the areas of potential taskforce activities, and recommend the taskforce team formation to the Technical Committee
        - Handle any type of 3 dimensional IC package technologies including fan-out wafer level package or integrated SiP.
        - Provide the communication link from all layer of supply chain in Japan.
        - Interact with North America and Taiwan Technology Committee for the joint programs planning.
- Workshops for 3DS-IC Standardization
  - 1st Workshop
    - Held on Sept. 7, 2015 at SEMI Japan office
    - More than 60 attendees
    - Yole, ITRI, Tokyo Seimitsu and Toray Engineering made presentations
  - 2nd Workshop
    - Held on January 12, 2016 at SEMI Japan office
    - More than 60 attendees
    - Yole, Otsuka Electronics and Hitachi Chemical made presentations
  - 3rd Workshop
    - Held on June 6, 2016 at SEMI Japan office
    - More than 60 attendees
    - Fukuoka IST, Tohoku University and Toray Engineering made presentations
- Other 3DS-IC related activities in Japan
  - Thin Chip Handling Task Force under Assembly & Packaging Japan TC Chapter
    - New Standard: SPECIFICATION FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
      - Doc. 5835 was published as SEMI G97-0116 in January 2016
      - SNARF for Line Item Revision to SEMI G97-0116 (Doc. 6028) and the ballot submission were approved at the next Assembly & Packaging Japan TC Chapter on June 10, 2016
    - Doc. 5836: New Standard: TEST METHOD FOR ADHESIVE STRENGTH FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
      - Ballot draft to be prepared
- Staff Contact: Chie Yanagisawa (cyanagisawa@semi.org)

Attachment: [2016Liaison] 3DS-IC Japan

3.2 *Taiwan TC Chapter*

Laura Nguyen reported for the 3DS-IC Taiwan TC Chapter. The key items were as follows:

- 3DS-IC Committee
  - Established in 2011, Mission: Focus on standards for Testing and Middle-end process in the manufacture and test methods of 3DS-IC industry
- Organization Chart *{See attachment for Figure}*
- Leadership
  - Committee cochairs: Wendy Chen (King Yuan Electronics), Roger Hwang (ASE)
    - New cochair: Chien-Chung Lin (ITRI)
    - The original co-chair Dr. TK Ku quit from ITRI and the new co-chair from ITRI is Dr. Chien-Chung Lin. This was approved by TC committee members in the last TC meeting that was held on May 5, 2016
- 3DS-IC Standard Committee Highlights
  - New standard passed technical and A&R review
    - Doc #5688A : 10/6/2015
    - Middle-end Process TF: "New Standard: Guide For Overlay Performance Assessment For 3DS-IC Process"
  - Doc #5800 ballot-drafting to be completed by the end of Q3 (target)
    - Middle-end Process TF: "New Standard: Guide for Wafer Edge Trimming for 3DS-IC Process "
- Meeting Information
  - Last meeting – SEMI Taiwan, May 5, 2016
  - Next meeting – SEMI Taiwan, September 8, 2016
- Staff Contact: Dean Chang (dchang@semi.org)

Attachment: [2016Liaison] 3DS-IC Taiwan

3.3 *SEMI Staff Report*

Laura Nguyen (SEMI) gave the SEMI Staff Report. The key items were as follows:

- SEMI Global 2016 Calendar of Events
  - SEMICON West (July 12-14, 2016, San Francisco, California)
  - SEMICON Taiwan (September 7-9, Taipei, Taiwan)
  - SEMICON Europa (October 25-27, Grenoble, France)
  - SEMICON Japan (December 14-16, Tokyo, Japan)
- Upcoming North America Standards Meetings
  - NA Standards Fall 2016 Meetings (November 7-10, 2016, SEMI HQ in San Jose, California)
  - NA Standards Spring 2016 Meetings (April 3-6 at SEMI HQ)
  - SEMICON West 2016 (July 10-13, 2017, San Francisco, California)
- Letter Ballot Critical Dates for 2016
  - Fall 2016 adjudication
    - Cycle 6: ballot submission due: July 22/Voting Period: August 1 – September 1
    - Cycle 7: ballot submission due: August 17/Voting Period: August 31 – September 30
  - Spring 2017 adjudication
    - Cycle 8: ballot submission due: Oct 17/Voting Period: Oct 24 – Nov 23
    - Cycle 9: ballot submission due: Nov 16/Voting Period: Nov 30 – Dec 30

- Standards Publications Report

Cycle	New	Revised	Reapproved	Withdrawn
December 2015	2	20	4	0
January 2016	0	8	10	0
February 2016	2	3	0	0
March 2016	0	4	3	0

  - Total in portfolio – 964 (includes 141 Inactive Standards)
- New Requirements/Process Reminders for TC Chapter Meetings
  - Standards Document Development Project Period
    - Project period shall not exceed three years (*Regulations* ¶ 8.3.2).
      - SNARF approval to TC Chapter approval
    - If Document development activity is found to be continuing, but cannot completed within the project period, TC Chapter may grant one-year extension at a time, as many times as necessary.
  - SNARF Review Period
    - A submitted SNARF for a new, or for a major revision to an existing, Standard or Safety Guideline is made available to all members of a TC Chapter's parent global technical committee for two weeks for their review and comment. (*Regulations* ¶ 8.2.1).
      - If the SNARF is submitted at a TC Chapter meeting, the TC Chapter can review and approve, but the SNARF will need to be distributed for two weeks and then approved via GCS.
  - New SNARF & TFOF forms *{embedded in Staff Report, see the attachments of these minutes}*
  - Procedures for Correcting Nonconforming Titles of Published Standards Document (*Procedure Manual* Appendix 4)
    - Some Standards qualify for a special procedure where a line-item change can be used to correct the titles. Otherwise, the corrective action will likely require a major revision.
    - None
  - 3DS-IC Standards needing Five-Year Review
    - None
  - SNARF 3 Year Status
    - Doc. 5173, New Standard: Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack
      - SNARF was approved on 3/29/2011
      - Granted 1 year extension in March 2015 meeting
      - Granted additional year in Spring 2016
      - Action needed by Spring 2017
    - Doc. 5822, New Standard: Specification for Reference Material for Bonded Wafer Stack Void Metrology
      - SNARF was approved on 11/4/2014
      - Action needed by West/Fall 2017
      - Work on-going
    - TC Chapter may grant a one-year extension
- Staff Contact: Laura Nguyen (lnguyen@semi.org)

Attachment: SEMI Standards Staff Report

4 Ballot Review

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.

Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

NOTE 2: TC Chapter adjudication on ballots reviewed is detailed in the Audits & Review (A&R) Subcommittee Forms for procedural review. The A&R forms are available as attachments to these minutes.

4.1 Document # 5713A, New Standard: Specification For Glass Base Material For Semiconductor Packaging

- The ballot passed as balloted. See attachment for ballot adjudication.

Attachment: ProceduralReview5713A

5 Subcommittee and Task Force Reports

5.1 *Bonded Wafer Stacks Task Force*

Richard Allen reported that there is no new activity aside from the ballot review for Doc 5713A. The task force reviewed the ballot results for Doc 5713 and can be found in Section 4 of these minutes. The task force presented two new SNARFs to the committee for review and made modifications. The key items are as follows:

Motion:	To submit SNARF, New Standard: Guide for Describing Glass-Based Material for Use in 3DS-IC Process, for document number, on contingent approval after two-week TC member review and GCS approval.
By / 2nd:	Steve Martell (Sonoscan) / Bevan Wu (BW & Associates)
Discussion:	None.
Vote:	5-0 in favor. Motion passed.

Attachment: SNARF-Glass Guide edits 20160712

Motion:	To submit SNARF, New Standard: Specification for Identification and Marking for Bonded Wafer Stacks, for document number, on contingent approval after two-week TC member review and GCS approval.
By / 2nd:	Steve Martell (Sonoscan) / Mark Takahashi (Asahi Glass)
Discussion:	None.
Vote:	5-0 in favor. Motion passed.

Attachment: SNARF-Wafer Marking edits 20160712

5.2 *Inspection & Metrology Task Force*

Richard Allen reported for the Inspection & Metrology Task Force. A few things that they went over was the presentation of IPC update below, pending memorandum, and the MEMS bond void survey results that can be found in the new business section 7.1.

5.2.1 IPC Update

Steve and Vern presented the IPC Update presentation. The key items from the PowerPoint were as follows:

IPC-7091
Design and Assembly Process Implementation of 3D components
Working Draft Development

Working Group Chair: Dudi Amir, Intel Corp.

Working Group Vice Chair: Vern Solberg

IPC Staff Support: Chris Jorgrnsen

- This document describes the design and assembly challenges for implementing 3D component technology.
- We understand that the effect of combining multiple uncased semiconductor die elements in a single package format can impact individual component characteristics and can dictate suitable assembly methodology.
- The focus of the information contained herein is on achieving optimum functionality, process assessment, repair, and reliability issues associated with 3D semiconductor package assembly and processing.
- The intent is to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation.
- The 3D semiconductor package may include multiple die elements, which can be homogeneous or heterogeneous.

The package may also include several discrete passive surface mount technology (SMT) devices as well as some that are integrated (embedded) within the component substrate structure.

- Project History-
  - Feb 2015 — Planning meeting, IPC Apex/Expo, San Diego, CA
  - Apr 1 and 2 2015 — Interim working meeting, Promex facility, Santa Clara, CA
  - July 22, 2015 — Interim working meeting, Intel Facility, Hillsboro, OR
  - Sep 30, 2015 — IPC Fall Meeting, Stevens Conv. Ctr., Rosemont, IL
  - Dec 2nd 2015 — Interim working meeting (Teleconference)
  - Jan 27 2016 — Interim working meeting (Teleconference)
  - Mar 16, 2016 — IPC Apex/Expo 2016, Las Vegas Conv. Ctr., Las Vegas, NV
  - Apr 27, 2016 I — Interim working meeting (Teleconference)
  - Jun 1, 2016 — Interim working meeting (Teleconference)
  - Jul 11, 2016 — Interim working meeting, Promex facility, Santa Clara, CA
  - Jul 20, 2016 — Interim working meeting, AXIOM, Beaverton, OR
  - **Spring 2017** — **Targeted publication**
- *{See attachment for images of 3D Die Stack, 3D Package-on-Package, 3D w/HDI Interposer, 3D System-in-Package, 3D Imbedded Component Substrate}*
- The document will furnish an overview for four substrate interposer variations: Organic, Silicon, Glass, Ceramic
- Information will include substrate interposer via hole forming and plating processes as well as methodologies for conductor metalization.
- Organic-Based Interposer Design:
  - Blind an buried micro vias
  - Fine-line build-up technology
- Silicon-Based Interposer Design
  - Through Silicon Via (TSV) Formation
  - Circuit metalization process variations
- Glass-Based Interposer Design
  - Through Glass Via (TGV) Formation
  - Circuit metalization process variations

- Ceramic-Based Interposer Design
    - Via ablation and plating/filling
    - Circuit metalization process variations
- Assembly of 3D Packages on PCBs
    - 2D and 3D Package structures
    - In-Package joining methods
    - Care and handling (ESD precautions)
    - Solder processing and reinforcement methods
- Inspection and Failure Analysis
    - Non Destructive methodologies
        - Optical inspection
        - 3D X-Ray analysis
        - Ultrasonic acoustic imaging
        - CSAM (Acoustic Microscopy)
        - Infrared (IR) Thermography
        - Electrical Probing
    - Destructive FA methodologies
        - Cross Section
        - Parallel Lapping
        - Decapsulation (Decap)
- The 'Draft Copy for Review' is expected to be released before or soon after the IPC Fall Meeting in Rosemont, IL (25-29 September)
- Feedback from task group members and contributors typically takes two to three months
- Comments, editorial and technical, will be addressed during web meetings and/or at IPC APEX/EXPO in San Diego, CA in February

Attachment: IPC-7091 2016 Overview

6 Old Business

Previous action items have been closed. There is no further old business.

7 New Business

7.1 *MEMS Survey - Sealed MEMS Devices and Wafer Stacking*

A survey was sent out looking to gather information on how to help guide future standards activities. The results that were reported were very low, so the TC Chapter extended the survey through the month of June. Rich Allen and Bill Kerr presented the results of the bond void survey. Some highlights that were gathered showed that the results came back quite interesting. It was very diverse and the committee is deciding whether this is something to go back and answer since the responses did not seem to point to any particular trend. Either the sample was too small or too diverse, both in which would be interesting to know. There seems to be a fair amount of interest from responses received and they do seem concerned or interested. The committee will possibly send out a compilation of the results with feedback

and send it to the members of the 3DS-IC, MEMS/NEMS, and MSIG committees. Please see attachment for complete survey results.

Action Item: 2016July#01, Len and Bill to summarize survey results to redistribute to the members.

Action Item: 2016July#02, Laura and Rich to send email to winner of survey results.

Attachment: Bond Void Survey Results

7.2 *Flex Discussion*

Rich presented the idea of possibly a Flexible Hybrid Task Force under the 3DS-IC Committee as a starting point until it gathers enough support and expertise to move it into its own committee. Main topics from the discussion was the idea of where it would fit. To align flexible electronics under this committee, the scope or charter may need to be revised.

8 Next Meeting and Adjournment

The next meeting is scheduled for Tuesday, November 8, 2016 for the Fall North America 2016 Standards Meetings at the SEMI Headquarters in San Jose, California. See http://www.semi.org/en/events for the current list of meeting schedules.

Having no further business, a motion was made to adjourn. Adjournment was at 14:50.

Respectfully submitted by:
Laura Nguyen
SEMI International Standards Coordinator
Phone: +1.408.943.7019
Email: lnguyen@semi.org

Minutes approved by:

Richard Allen (NIST), Co-chair	November 8, 2016
Chris Moore (BayTech-Resor), Co-chair	<Date approved>
Sesh Ramaswami (Applied Materials), Co-chair	<Date approved>

Table 8 Index of Available Attachments[#1]

Title	*Title*
SEMI Standards Required Meeting Elements	ProceduralReview5713A
[2016Spring] NA 3DS-IC Minutes FINAL edits 20160712	IPC-7091 2016 Overview
[2016Liaison] 3DS-IC Japan	SNARF-Glass Guide edits 20160712
[2016Liaison] 3DS-IC Taiwan	SNARF-Wafer Marking edits 20160712
Staff Report June 2016 (3DS-IC)	Bond Void Survey Results

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Laura Nguyen at the contact information above.