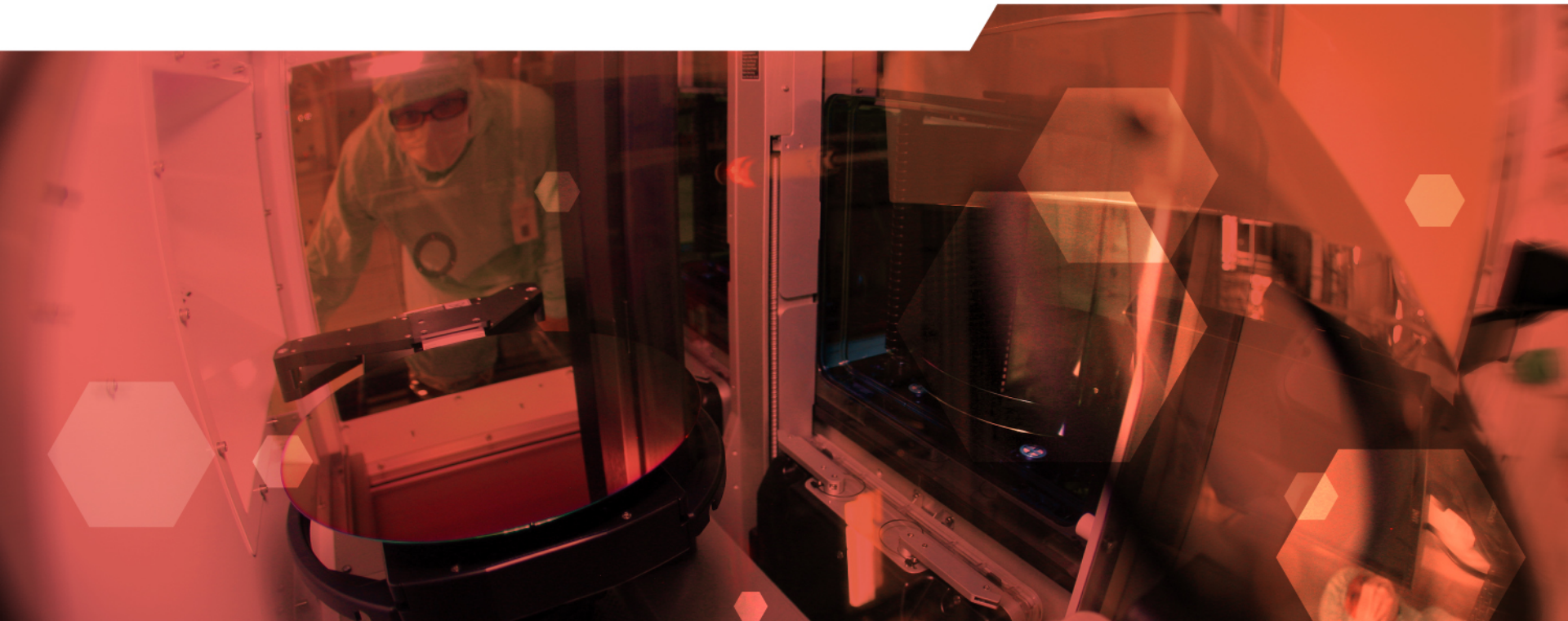


Taiwan TC Chapter 3D Packaging & Integration (3DP&I) Global Technical Committee

Liaison Report

March 2019

v1



Meeting Information

- Last meeting
 - March 26, 2019 at the SEMI Standards Taiwan Spring 2019 Meetings
 - SEMI Taiwan Office, Zhubei City, Hsinchu County, Taiwan
- Next meeting
 - June 6, 2019 at the SEMI Standards Taiwan Summer 2019 Meetings
 - SEMI Taiwan Office, Zhubei City, Hsinchu County, Taiwan

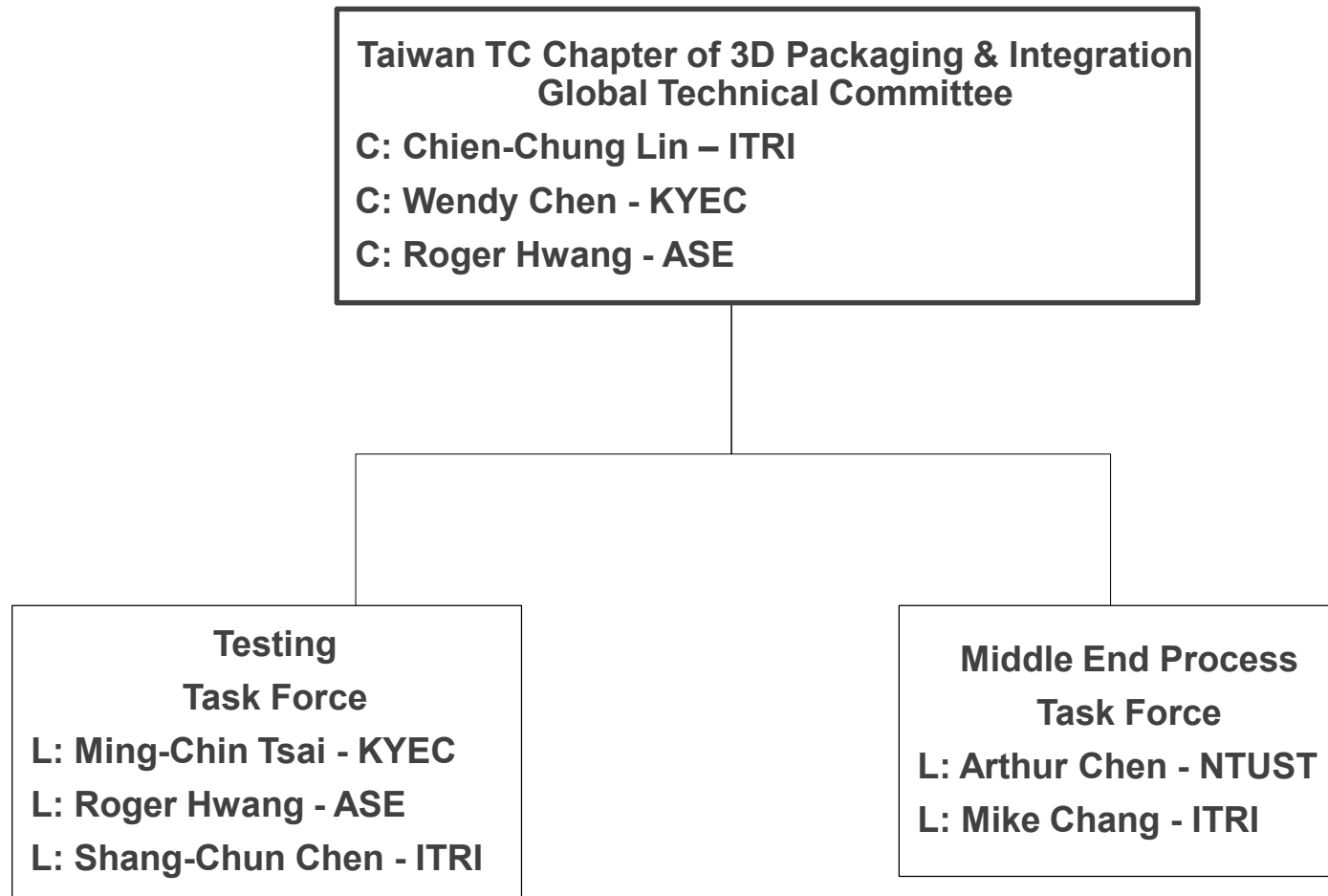
<http://www.semi.org/en/standards-events>

Leadership

Co-chairs

- Chien-Chung Lin - ITRI
- Wendy Chen - King Yuan Electronics Company
- Roger Hwang - ASE

Organization Chart



Ballot Results

Doc #	Document Title	TC Chapter Action
5008A	New Standard: Guide for Wafer Edge Trimming for 3DS-IC Process	Passed , ISC A&R SC on 2018/07/06
6405	Reapproval of SEMI 3D7-0913, GUIDE FOR ALIGNMENT MARK FOR 3DS-IC PROCESS	Passed , ISC A&R SC on 2018/10/19
6411	Line Item Revision of SEMI 3D6-0913 Guide for CMP and Micro-bump Processes for Frontside Through Silicon Via (TSV) Integration	Passed , forward to A&R for procedural review

Note 1: **Passed** ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.

Note 2: **Failed** ballots and line items were returned to the originating task forces for re-work and re-balloting or abandoning.

Abolished SNARF(s)

Doc #	TF	Title/Details
	Testing Task Force	<p>New Standards: Guideline for Chip ID registering and tracing</p> <p><i>– The scope of this SNARF is similar with SEMI T23-0119 “New Standard: Specification for Single Device Traceability for the Supply Chain” which was submitted by Traceability TC/ Single Device Traceability Task Force</i></p>

Task Force Highlights (1/2)

- 3DP&I Middle-End Process Task Force
 - #5800A: New Standard: Guide for Wafer Edge Trimming for 3DS-IC Process
 - Approved by A&R on 2018/07/06
 - Publication pending
 - #6405: Reapproval of SEMI 3D7-0913, GUIDE FOR ALIGNMENT MARK FOR 3DS-IC PROCESS
 - Approved by A&R on 2018/10/19
 - Publication pending
 - #6411: Line Item Revision of SEMI 3D6-0913 Guide for CMP and Micro-bump Processes for Frontside Through Silicon Via (TSV) Integration
 - Passed technical ballot Cycle 6-18 and forward to A&R for procedural review

Task Force Highlights (2/2)

- Testing Task Force
 - Studying the feedback of SNARF “New Standards: Guideline for Chip ID registering and tracing” from global TC members’ two weeks review
 - The scope of this SNARF is similar with SEMI T23-0119 “New Standard: Specification for Single Device Traceability for the Supply Chain” which was submitted by Traceability TC/ Single Device Traceability Task Force
 - Abolished this SNARF “SNARF “New Standards: Guideline for Chip ID registering and tracing”

Staff Contact

Thank you

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