3D Packaging & Integration Taiwan TC Chapter

Chang-Sheng Chen/March Chen, ITRI, 2021

3DS-IC Testing Task Force

- Statement
  - 5-year review:
    Guide for Incoming/outgoing Quality Control and Testing Flow for 3DS-IC Products (3D14-0615)
  - Study of Probe card Current Carrying Capability (CCC) standard assessment guideline

Over 5 years review
SEMI 3D14-0615

Guide for Incoming/outgoing Quality Control and Testing Flow for 3DS-IC Products

IQC / OQC Testing Flow

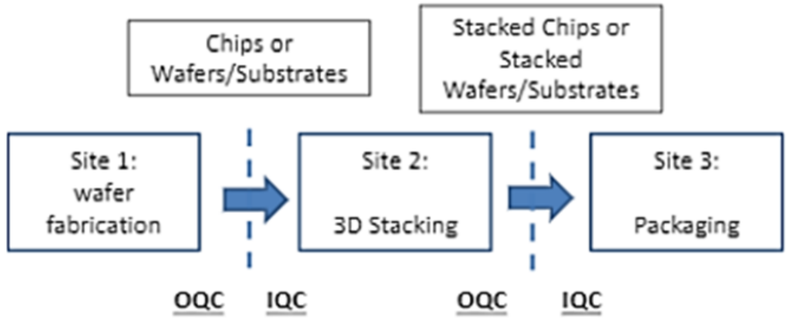


Figure 1Figure 1
The IQC and OQC are Required in the 3DS-IC Manufacturing Flow Where the Product is in the Form of Semi-Finished Good and a Site to Site Transfer Occurs

IQC:

Review of attached documents:

1. Device number
2. Lot number
3. Wafer pieces
4. Chip quantity
5. Wafer size
6. Mask code
7. Wafer thickness
8. Wafer identification
9. Flat/notch direction
10. Wafer type
11. Chip type
12. Pad/bump/pillar material
13. Pad/bump/pillar structure
14. Summary report including AOI data

Review of product

1. Visual inspection
2. Optical microscopy inspection

OQC:

Review of product and summary report:

1. Check for mechanical and structural defects
2. Check for process defects
3. Check pad contamination, silicon residue in the product
4. Ink inspection

Review of attached documents

1. Box label
2. Testing reports
3. Product OQC inspection summary reports

Shipping product quantities

Packaging inspection

IQC / OQC Testing Flow

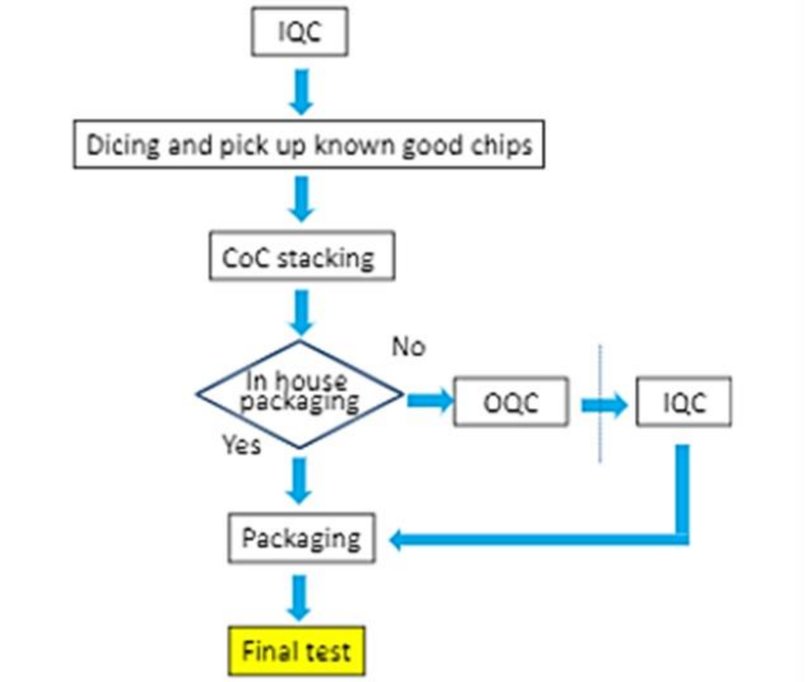


Figure 2
The Testing Flow of CoC (Chip on Chip) Stacking

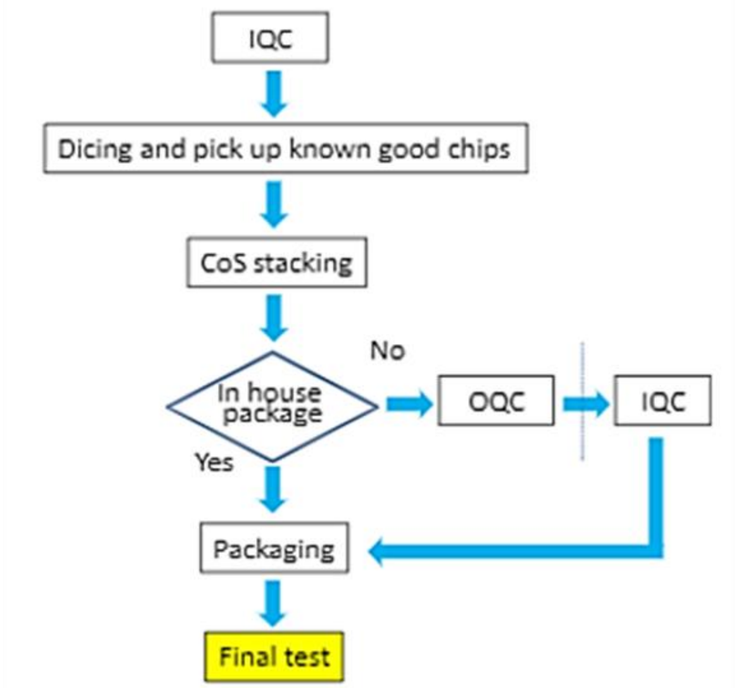


Figure 3
The Testing of CoS (Chip on Substrate) Stacking

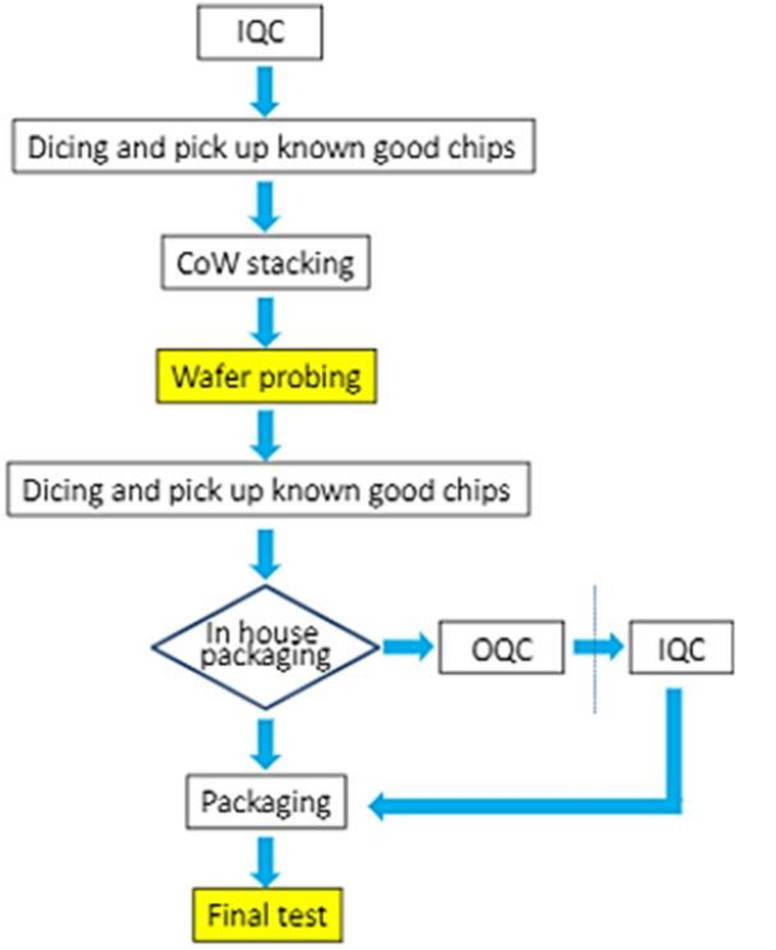


Figure 4
The Testing Flow of CoW (Chip on Wafer) Stacking

IQC / OQC Testing Flow

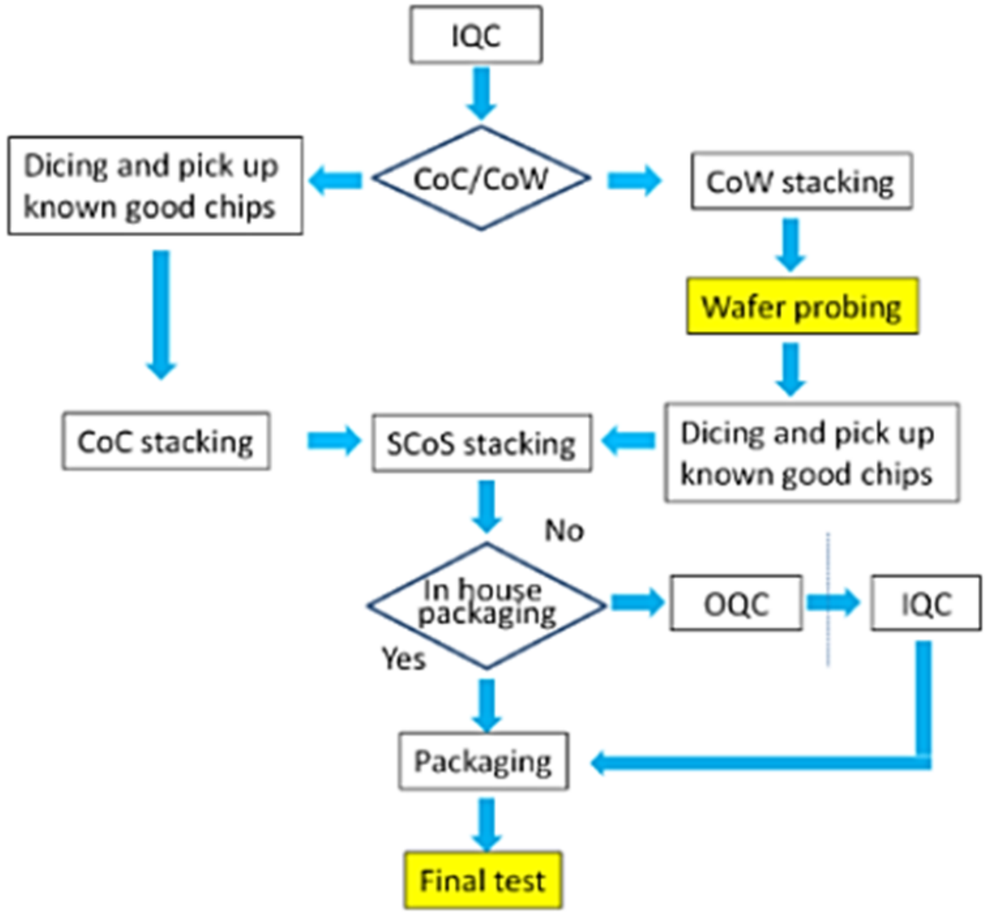


Figure 5
The Testing Flow of SCoS (Stacked Chip on Substrate) Stacking

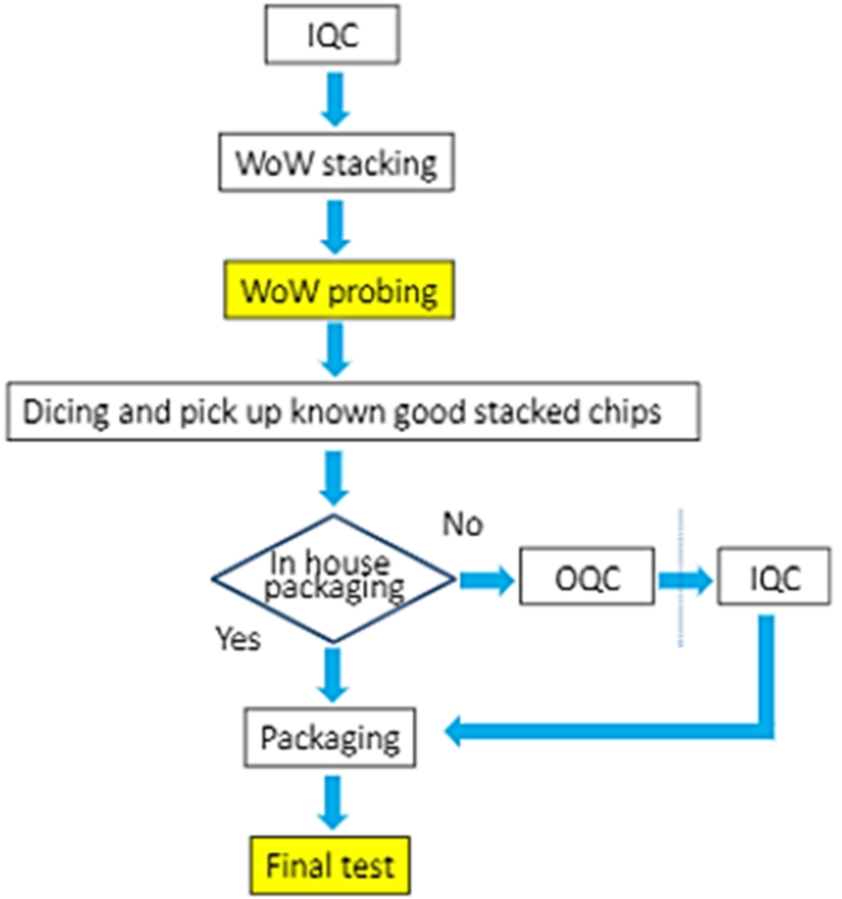


Figure 6
The Testing Flow of WoW (Wafer on Wafer) Stacking

TF Meeting Minutes

TF meeting discussion
Date/time: June 24, 14:00-15:00
Venue: on-line meeting
Attendee: Roger Hwang, Chang-Shen Chen, Clark Liu, March Chen, Henry Lee, Ada Tai

Conclusion:
Upheld the standard with the modification below:

7 IQC

7.1 This section defines the IQC criteria of 3DS-IC products. The 3DS-IC product, either stacked chips or wafers, and the documents attached

7.2 *Review of Attached Do* map information which are

7.2.1 Documents checklist:

1. Device number
2. Lot number
3. Wafer pieces
4. Chip quantity
5. Wafer size
6. Mask code
7. Wafer thickness
8. Wafer identification
9. Flat/notch direction
10. Wafer type: unbond or bonded, single or double
11. Chip type: single chip or stacked chip
12. Pad/bump/pillar material: Al, Au, etc.
13. Pad/bump/pillar structure
14. Summary report including AOI data

9. Flat/notch direction
10. Wafer type: unbond or bonded, single
11. Chip type: single chip or stacked chip
12. Pad/bump/pillar material: Al, Au, etc.
13. Pad/bump/pillar structure

Add wafer notch and metal structure description

8 OQC

8.1 This section defines the OQC criteria of 3DS-IC semi-finished goods, such as stacked chips for further stacking or final molding. The 3DS-IC product, no matter stacked chips or wafers, and the documents attached to describe this product are examined separately in the OQC process.

8.2 *Review of Product and Summary Report* — The review of the out-going goods should include the inspections of the following defects listed below and summarized in the report.

8.2.1 Check for mechanical and structural defects, such as scratches, chips, and breaks in the product.

8.2.2 Check for process defects such as missing ball, bridging, and abnormal probing marks in the product.

8.2.3 Check pad contamination, silicon residue in the product.

~~8.2.4 *Ink Inspection* — Check that any required ink identification on the product is existing and intact.~~

Delete ink inspection

Study of Probe card Current Carrying Capability (CCC) standard assessment guideline

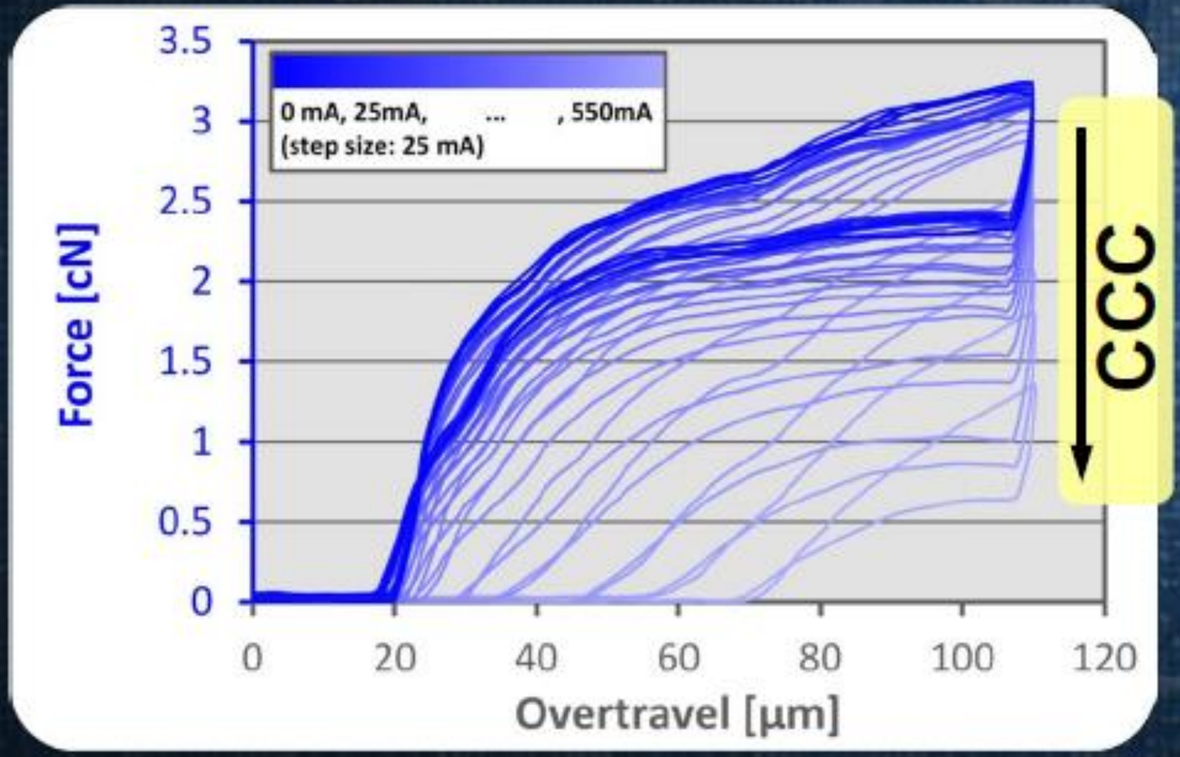
SEMI 3DS-IC Testing Task Force

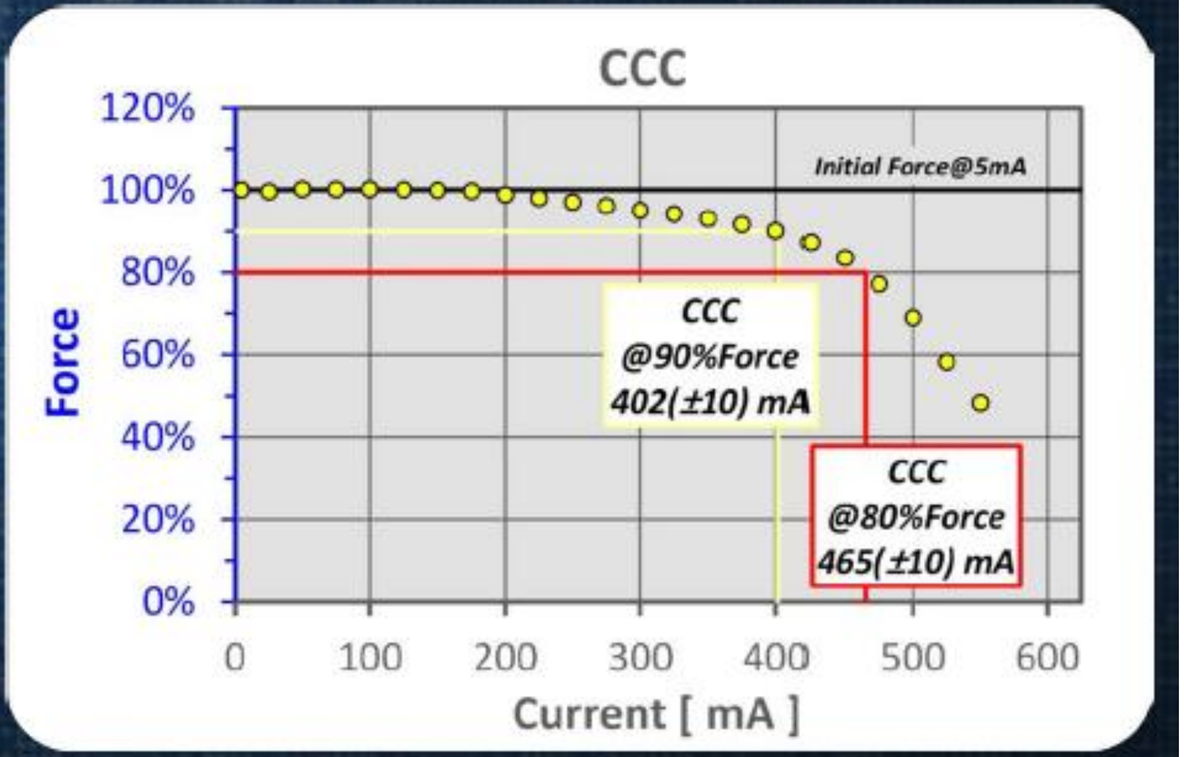
Methods

- **Current Carrying Capability – Main Presentations**

Methods

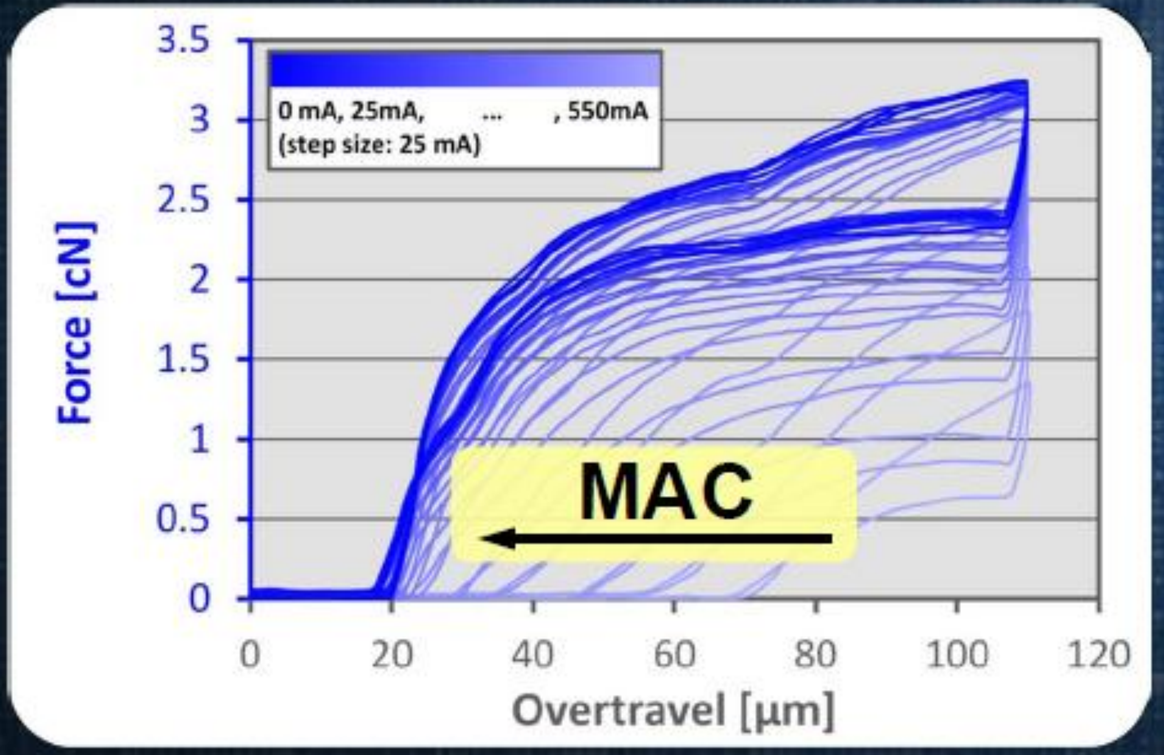
- **Better and More Comparable Method**

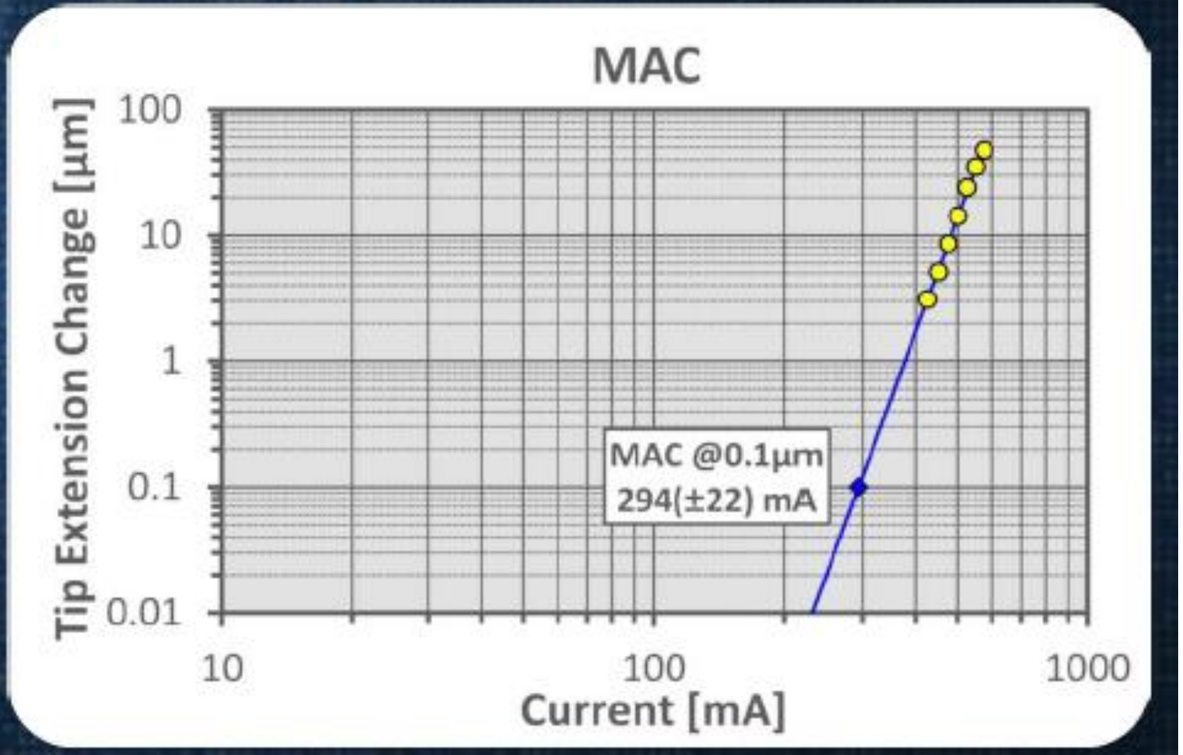




Methods

- **Better and More Comparable Method**





Meeting Minutes

2021/4/7

1. PTI shares the experience about the insufficiency of probe card CCC definition, and recommends to add MAC to control the unexpected failure issue. All members agree this scope direction and have the consensus to make a MAC guideline.

2021/6/7

1. KYEC MT Tsai shares user experience.

2. Make consensus to proceed the “MAC guideline for probe card” as standard for TC meeting review.

3. Testing method is not distinct in the current publications, need to be identify in the future.

Action: probe card vendors to provide the detail testing method recommendation in next discussion meeting (roughly to be scheduled after 3 months, SEMI staff will call in Aug.).

4. Next Meeting will be September/M

IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

June 7-10, 2009
San Diego, CA

ISMI Probe Council

Current Carrying Capability Measurement Standard

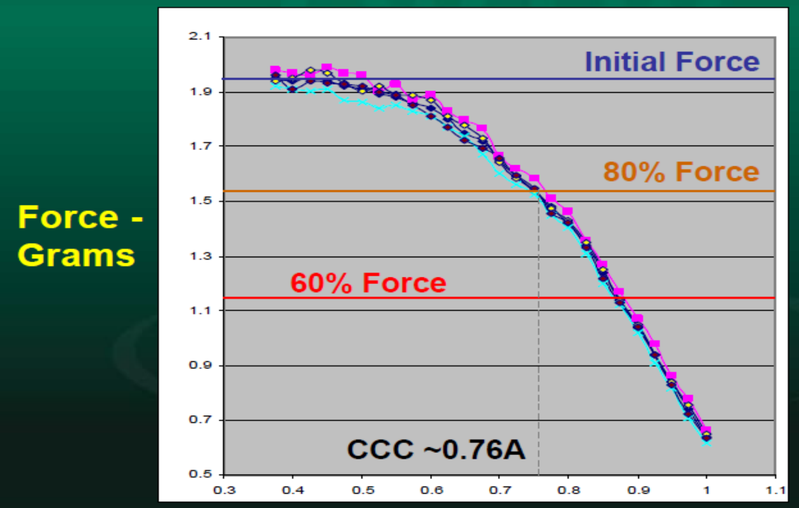
E Boyd Daniels
Probe Council Chairman
Texas Instruments

INTERNATIONAL SEMATECH ISMI MANUFACTURING INITIATIVE

Measurement Conditions

- **The fail signature chosen for the CCC value is a permanent reduction of force in the probe.**
- **By measuring the point at which this force is reduced by 20% for nominal overdrive settings, good electrical contact is still temporarily maintained.**
- **However, the robustness of the contact has changed dramatically and further use in production may lead to higher maintenance and eventual loss of contact.**

Method



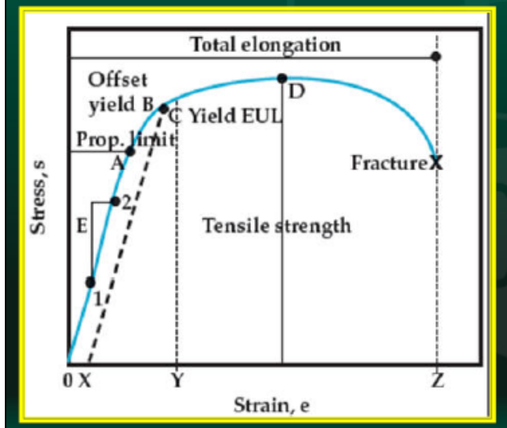
- ISMI 耐電流定義能找出造成 “短時間” 造成探針形變電流值。
- 而目前測試廠面臨的是隨著 Touchdown次數增加 ，Probe Mark 逐漸變小，探針逐漸下陷的燒針狀況。
- 目前測試會導致探針下陷的平均通過單針電流值 ≈ 10% * ISMI CCC

Current Carrying Capability

- Current carrying capability (CCC) of a probe is defined as the maximum current which it can carry with reliable contact.
- Factors Affecting CCC:
  - Ambient Temperature
  - Contact Resistance
  - Probe Material
  - Probe Geometry
  - Wafer Temperature

Probe Loading at Room Temperature

- Before Current is Applied to the Probe, it is Overdriven to a Specified Amount
- This Overdrive Causes a Rise in Stress in the Probe ($\sigma \propto OD$)
- Probes are Designed to Remain in the Elastic/Recoverable Region to get Multiple Touchdowns (TDs)



Any time this rule is violated, the probe will deform permanently, causing severe life reduction & loss in probe height!

CCC

- Based on the proposed theory, CCC can be re-defined as:
  "The maximum current a probe can handle without permanently deforming (stresses remain below the yield strength) at its fully loaded state for repeated number of cycles."
- This definition ensures the probe never loses height or deforms permanently even with passage of max prescribed current.
- It also ensures the planarity of the card does not change with passage of current.

- 從2010 SV Probe 的觀點中，探針保持彈性形變才能保證連續的 Touchdown。
- **若探針承受應力 > 探針Yield Stress，就會造成針下陷(永久形變).**

STANDARDS NEW ACTIVITY REPORT FORM

Refer to *Procedure Manual* § 2.2.4 for more information on properly filling out the SNARF.

1. Rationale:

a: Describe the need or problem addressed by this activity.

(Indicate the customer, what benefits they will receive, and if possible, quantify the impact on the return on investment [ROI] if the Document is implemented.)

有鑑於3DIC堆疊晶片數量越來越多且日益複雜，衍生出stacked cube, chiplet等多晶片整合在電路板上，在測試時容易遇到瞬間總電流量超出預期時(例如晶片短路造成大電流、多級晶片操作下使電流放大超出限制等)，易使探針超出可承受的電流而損壞。

現有探針對承受電流的選用常依據ISMI CCC spec，但仍常發生操作在低於此規格之電流仍然燒針的問題，因此需要制定新的guideline提供user參考。

2. Scope:

a: Describe the technical areas to be covered or addressed by this Document development activity.

(For Subordinate Standards, list common concepts or criteria that the Subordinate Standard inherits from the Primary Standard, as well as differences from the Primary Standard.)

擬訂定一guideline，在user欲測試複雜度較高的堆疊晶片時作參考：探針或探針卡產品除了提供CCC(current carrying capability)測試數據外，再加註最大容許電流(maximum allowable current, MAC)規格，以及揭露MAC的測試參數。可提供設計者及測試者，在設計電路、撰寫測試程式及選用探針時，預先依此MAC作保護考量，一般來說MAC數值低於CCC，操作於MAC下可有效避免測試時因複雜晶片或不可預期電路問題而產生的大電流將探針燒壞，藉此可增加測試效率及探針的壽命。

(MAC的測試方法可依廠商及產品而定，不在此guideline範圍)