3D Packaging & Integration Taiwan TC Chapter

WH Lin, Mike Chang, ITRI, 2021

3DP&I Middle-End Process Task Force

- Statement
  - Over 5 years review
    - SEMI 3D15-0316 Guide for overlay performance assessment for 3DS-IC process
  - New topic direction discussion
    - CMP Standard for hybrid bonding

Over 5 years review
SEMI 3D15-0316

Guide for overlay performance assessment for 3DS-IC process

Terminology and Definition

5.1.1 *CMP* — chemical mechanical planarization

5.1.2 *DOF* — depth of focus

5.1.3 *F2B* — face to back

5.1.4 *F2F* — face to face

5.1.5 *IR* — infrared

5.1.6 *OM* — optical microscopy

5.1.7 *TIS* — tool induced shift

5.1.8 *W2W* — wafer to wafer

5.2.1 *centerline* — a reference line that is equidistant from opposite edges of a feature.

5.2.2 *feature* — area within a single continuous boundary that have any physical property that is distinct from the background area outside the feature. (See Figure 4.)

5.2.3 *offset direction* — overlay vectors should be decomposed into orthogonal components, *X* and *Y*, along the directions of the stepper stage motion, and a rotation angle θ calculated by *X* and *Y* offset values. *X* Direction is positive to the right, *Y* Direction is positive to the up, Theta direction is positive counter clockwise, as indicated in the following figure. (See Figure 3.)

5.2.4 *overlay* — a vector quantity defined at every point on the wafer. It is the difference, $\overline{O}$, between the vector position, $\overline{P}_1$, of a substrate geometry, and the vector position of the corresponding point, $\overline{P}_2$, in an overlaying pattern, which may consist of photoresist: $\overline{O} = \overline{P}_1 - \overline{P}_2$. (See Figure 1.)

5.2.5 *pattern* — a group of features for overlay metrology. (See Figure 4.)

5.2.6 *registration* — a vector quantity defined at every point on the wafer. It is the difference, $\overline{R}$, between the vector position, $\overline{P}_1$, of a substrate geometry, and the vector position of the corresponding point, $\overline{P}_0$, in a reference grid: $\overline{R} = \overline{P}_1 - \overline{P}_0$. (See Figure 2.)

NOTE 1: Note that overlay is a relative quantity, while registration is an error compared to an ab

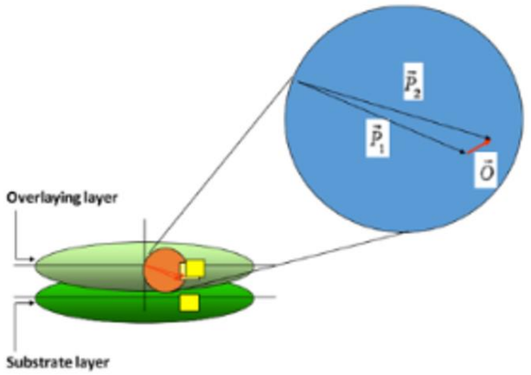


Figure 1
Schematic of Overlay Vectors

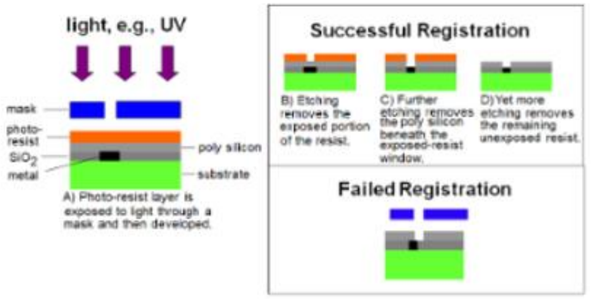


Figure 2
Schematic of Registration Processes
Left: Before Photolithography, Right: After Photolithography

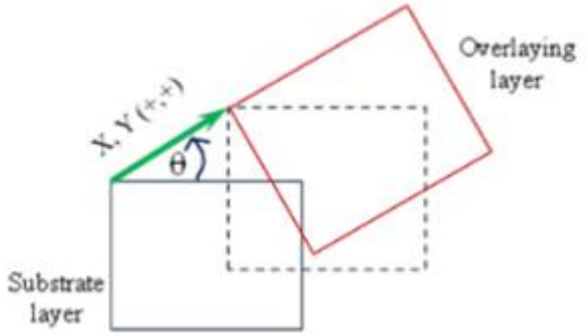


Figure 3
Overlay Vectors Definition

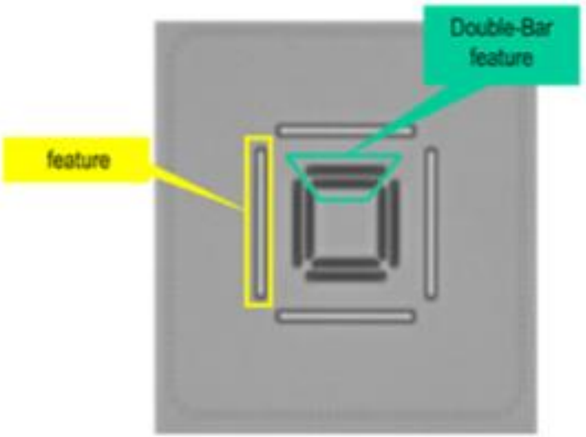


Figure 4
Features and Pattern

Sample and instrumentation general specification

- Overlay pattern design guideline
  - Represent in-circuit errors
  - robust to process circuit damages
  - not introduce new classes of error
  - practical to be printed in production conditions
  - Different patterns structures printed at different layer surface
  - Symmetric targets, Line edge space, Easy imaging by IR microscopy

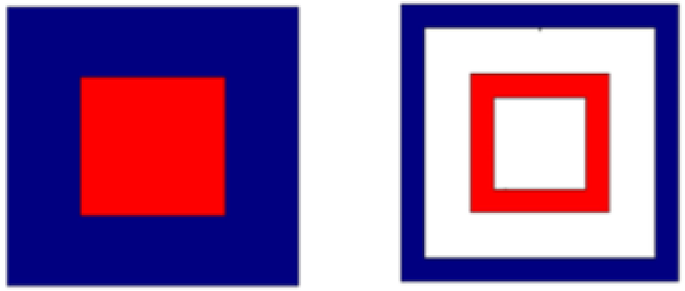


Figure 5
Examples of 90° Rotational Symmetry Pattern for Overlay Measurement

- Overlay measurement position guideline
  - Near device region
  - Minimum size: 10 um X 10 um for IR
  - Distinct in–chip pattern
  - Device scribe line (100 um wide)

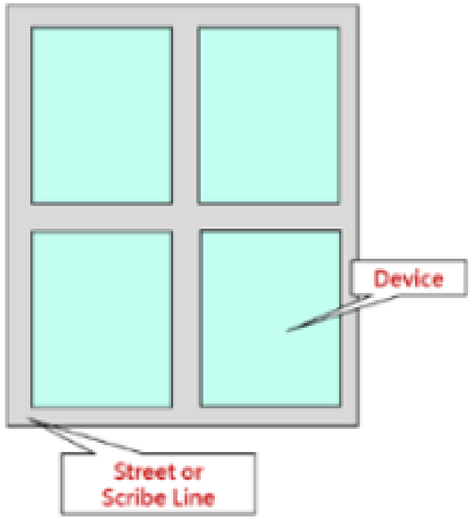


Figure 6
Schematic of Device Scribe Lines

- General instrument configuration
  - IR is possible capture images through bulk silicon for 3D interconnect metrology

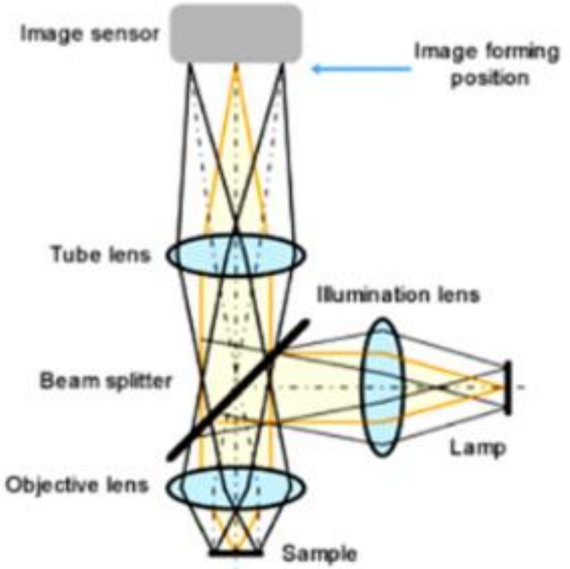


Figure 7
Generic Infrared Microscopy Configuration

Overlay performance assessment guideline

- Measurement algorithm
  - Face to face bonding
    - Single image for sufficient DOF
    - Multiple image when DOF is not enough
  - Face to back bonding
    - Multiple image for top and bottom wafer surface
    - Merged different Z location image for overlay offset
  - Overlay analysis algorithms
    - threshold
    - derivative
    - pattern recognition

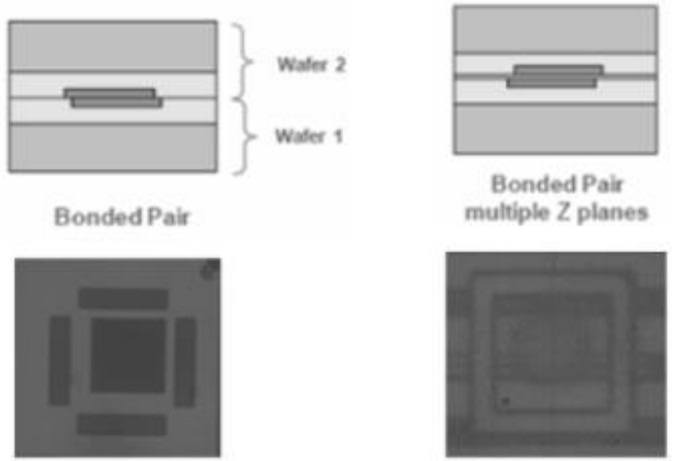


Figure 8
Schematic Diagram for F2F Measurement
Left: DOF is Sufficient, Right: DOF is not Enough

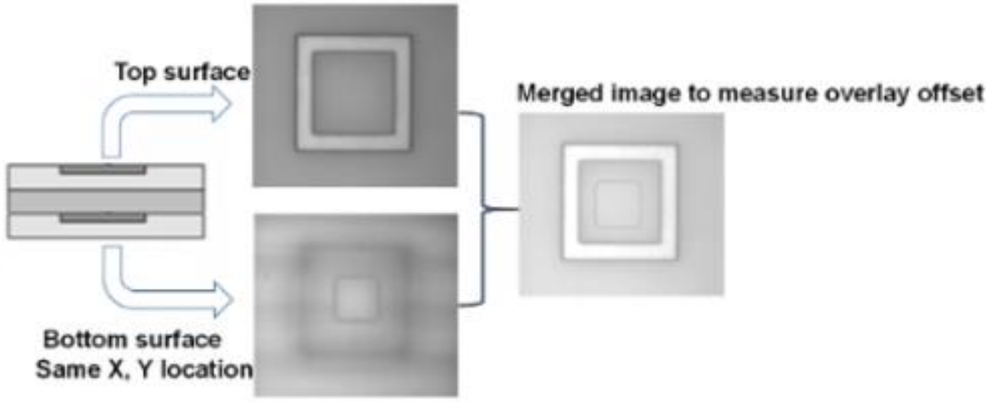
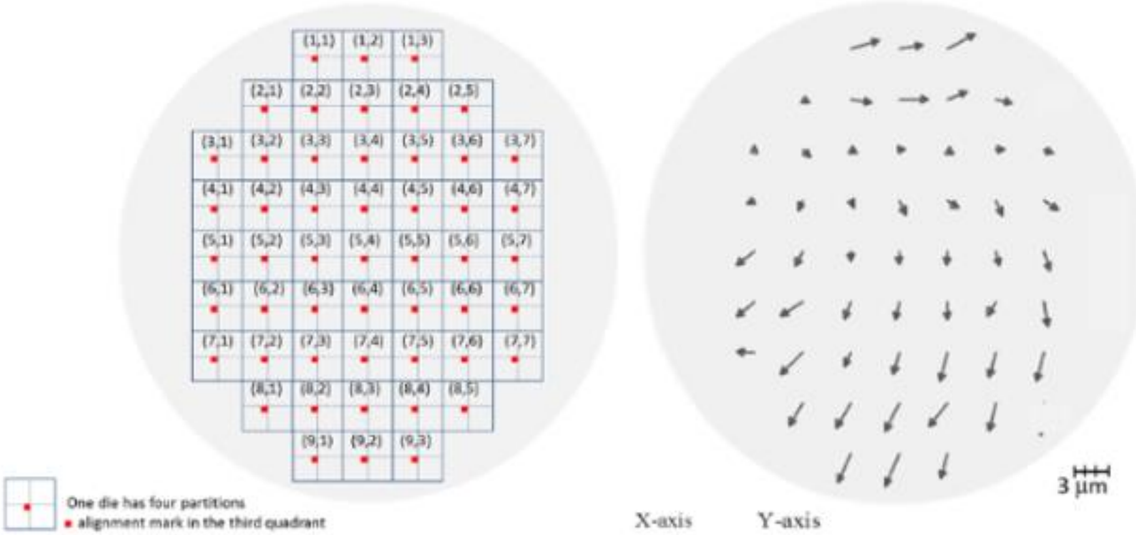


Figure 9
Schematic Diagram of Images Process for F2B Bonded Wafer Pairs

Overlay performance assessment guideline

- Analysis model
  - Liner model is used to describe the interfiled errors
  - ΔX and ΔY: X and Y directions overlay error
  - Tx and Ty: X and Y directions translation error
  - Ex and Ey: X and Y directions scale error (wafer expansion or contraction)
  - Rx and Ry: rotation factors
  - ex and ey: do not conform to the model
  - Typical display of measured overlay maps and statistic results

$$\Delta X = T_X + E_X X - R_X Y + e_X$$
$$\Delta Y = T_Y + E_Y Y + R_Y X + e_Y$$



	X-axis	Y-axis
Translation (μm)	0.04	-1.09
Expansion (ppm)	7.93	10.91
Rotation (μrad)	-14.16	-3.31
Residual (3σ) (μm)	1.79	1.29

Figure 10
Typical Display of the Measured Overlay Maps and Results from Linear Model Analysis

Overlay performance assessment guideline

- General cautions for applications
  - Matching error
    - More than one stepper is used
    - degree on to which the pattern placement produced on one stepper matches that of other steppers
  - Misregistration
    - Geometries on reticles results in overlay errors on wafers
    - Contributions that vary systematically across the reticles
  - Process dependent overlay effects
    - accuracy of alignment target depends upon the overall process
    - Film depositions, resist coatings, etches and polishes
  - Tool induced shift effects
    - overlay measurement metrology tool and method

- General cautions for applications
  - Tool induced shift effects
    - metrology tool induced systematic discrepancy in the overlay result due to the above system imperfections
    - A correctable error, three times the standard deviation of TIS measured over N sites across the wafer
    - TIS-variability reduction usually involves the improvements of the metrology tools and methods

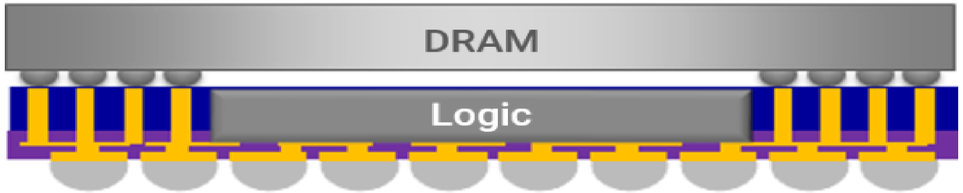
CMP Standard for hybrid bonding

Chiplet Integration

2021 Plan

- Different Process Node
- Different Wafer Size
- Lower Package Cost

Fan-Out



Chip to Chip

Issues

Handling

- Molding Wafer
- Glass Carrier
- Metal Carrier
- Total Thickness
- Warpage
- Thin Wafer Handling
- …

Process

- Micro-bump Process
- Hybrid Bonding
- Fine Line Process
- C2C/W2W Bonding
- Large Cu Pillar
- Chip Molding
- …

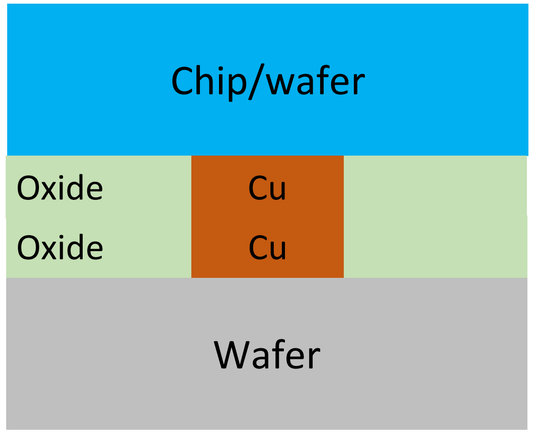
Testing

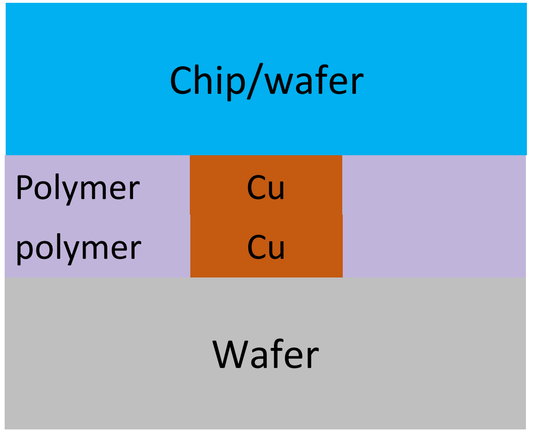
- Electrical Testing
- Particle Inspection
- Double Side Testing
- Die Tracing
- Module/System Testing
- Reliability Testing
- …

CMP Standard for hybrid bonding

- Cu hybrid bond
  - Surface condition:
    - STD/thin wafer bow/warp measurement
      - Allowance for process
    - Cu geometry (dishing/protruding) measurement
      - Thermal expansion volume vs pad size vs dishing depth
    - Surface roughness measurement
      - Allowance for bonding
  - Wafer type:
    - Si/Glass
  - Different application:
    - Mobile/Automobile

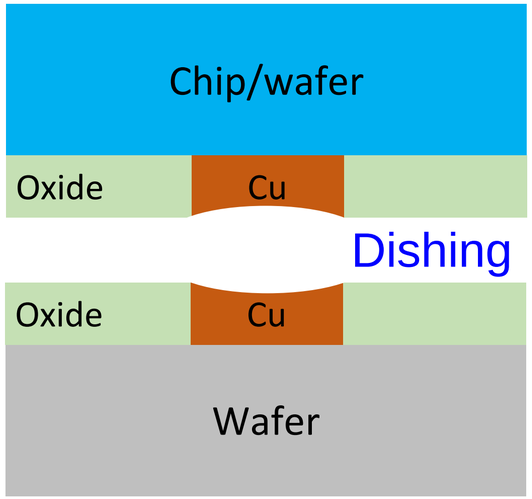
Hybrid bonding

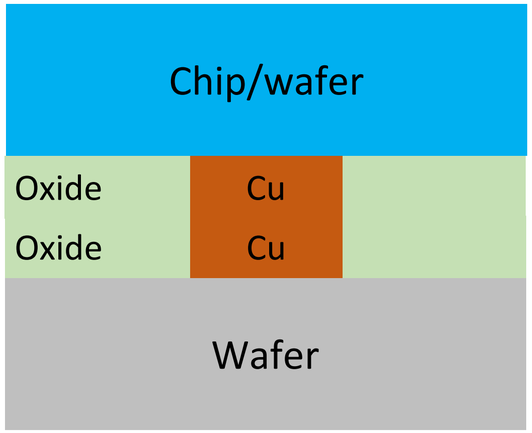




CMP Standard for hybrid bonding

Cu/oxide hybrid bonding

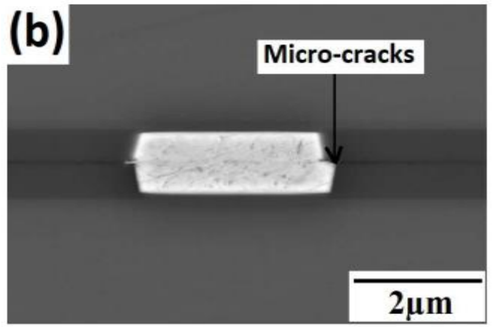




- Cu/oxide hybrid bonding
  - Surface roughness
  - Bump size/pitch
  - Dishing depth
  - Pattern density
  - layout

Recommended amount of Cu dishing

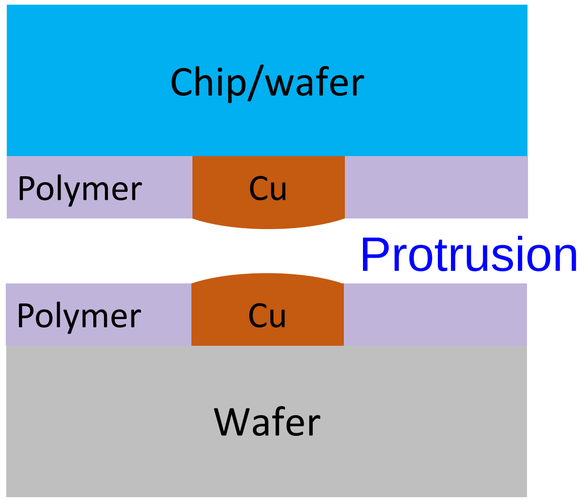
- Cu pad roughness < 2 nm, TEOS SiO_2 roughness < 0.5 nm.
- The preferred post-CMP Cu dishing value is 5-10 nm.
- Micro-crack generation in the dielectric zone external to Cu pads is high when the Cu dishing value is ≤ 5nm.
- The risk of voids generation at the Cu-Cu bond interface is higher when the Cu dishing value is ≥ 10 nm.

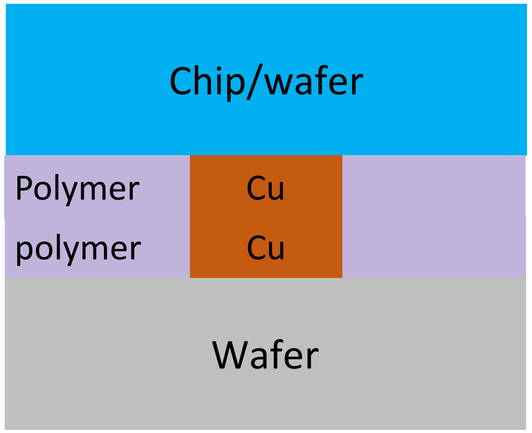


EPTC 2020, Wafer Level Fine-Pitch Hybrid Bonding: Challenges and Remedies

CMP Standard for hybrid bonding

Cu/polymer hybrid bonding





- Cu/polymer hybrid bonding
  - Surface roughness
  - Bump size/pitch
  - Protrusion height
  - Pattern density
  - layout

Recommended amount of Cu protrusion

- The height difference of Cu and PI caused by thermal expansion:
- $\Delta L = L_0 \Delta\alpha \Delta T$
- $= (3 * 10^3\ nm) * [(33 - 16.6) * 10^{-6}] * (200 - 25) = 8.61nm$
- CTE:
  - Low cured PI : 33 ppm/℃ (**full cured**)
  - Cu : 16.6 33 ppm/ ℃
- For a 3 μm thickness of Cu/PI structure, Cu should be at least 10 nm higher than PI