Silicon Wafer Committee
EU Chapter Meeting Summary and Minutes

SEMICON Europa
8 October 2014
Grenoble, France

Next Committee Meeting
October 2015
SEMICON Europa, Dresden, Germany

Committee Announcements (optional)

Table 1 Meeting Attendees

Co-Chairs: Peter Wagner (Self)
SEMI Staff: Andrea Busch, James Amano

Company	*Last*	*First*	*Company*	*Last*	*First*
Intel	Goldstein	Mike	Tokyo Electron	Mashiro	Supika
Consultant	Yoshise	Masanori	G450C	Lin	Pinyen
Siltronic	Passek	Fritz	SUMCO	Nakai	Tetusya
Consultant	Poduje	Noel	KLA Tencor	Sinha	Jaydeep
Intel	Goldstein	Mike			

Table 2 Leadership Changes

None

Table 3 Ballot Results

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

Document #	*Document Title*	*Committee Action*
5403	Withdrawal of SEMI MF534-0707, TEST METHOD FOR BOW OF SILICON WAFERS	**Passed as balloted**
5604	Line Item Revision to SEMI M1-0414 SPECIFICATIONS FOR POLISHED SINGLE CRYSTAL SILICON WAFERS and SEMI M20-1110 PRACTICE FOR ESTABLISHING A WAFER COORDINATE SYSTEM	**Passed as balloted**
5702	Line Item Revision to SEMI M68-1109, PRACTICE FOR DETERMINING WAFER NEAR-EDGE GEOMETRY FROM A MEASURED HEIGHT DATA ARRAY USING A CURVATURE METRIC, ZDD	**Passed with editorial changes**

Table 4 Authorized Ballots

#	When	SC/TF/WG	Details
5736	Cycle 7-2014	International SOI Wafers Task Force	Line Item Revision to M41-1213 Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

Table 5 Authorized Activities

#	Type	SC/TF/WG	Details
5794	SNARF	International 450 mm Wafer Task Force	New Standard: Specification Of Developmental 450mm Diameter Polished Single Crystal Notchless Silicon Wafers With Back Surface Fiducial Marks

Note: SNARFs and TFOFs are available for review on the SEMI Web site at:
http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 6 New Action Items

None

Table 7 Previous Meeting Action Items

None

1 Welcome, Reminders, and Introductions

Peter Wagner called the meeting to order at 13:30. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

2 Review of Previous Meeting Minutes

The committee reviewed the minutes of the previous meeting from SEMICON Europa 2013.

Motion: To approve the minutes as written.
By / 2nd: Jaydeep Sinha/Frank Riedel
Discussion: None
Vote: 8-0

3 Liaison Reports

3.1 *North America Chapter*

James Amano reported. Of note:

- International 450mm Task Force
  - eliminating the notch and replacing it with backside fiducial marks
  - reducing the edge exclusion zone from 2mm to 1.5mm.
  - Concerns of the fiducial and T7 marks penetrating in the exclusion area were discussed
  - Change in EE Will have to wait for M1 revision which includes notchless wafer introduction.
- Presentations:
  - Monitoring Process-induced Wafer Distortions in Advanced CMOS nodes (Oleg Gluschenkov/IBM)
  - Role of Process-Induced Wafer Geometry in Advanced Semiconductor Manufacturing (Kevin Turner/University of Pennsylvania)
- Int'l Advanced Wafer Geometry TF
  - Aligning ITRS and SEMI: Not much happening at ITRS which is going through lot of changes. Not much to expect in the immediate future form ITRS.

Attachment: NA Si Wafer Liaison Report 20140903.ppt

3.2 *Japan Chapter*

Tetsuya Nakai reported for the Japan Chapter. Of note:

- International 450mm Shipping Box Task Force
    - (Previous Leader) Yasuhiro Shimizu/ Shimizu Consulting
    - (New Leader) Shoji Komatsu/ Acteon
        - *Approved by GCS of the Silicon Wafer and PIC on August 20
- JA Shipping Box Task Force
    - (Previous Leader) Yasuhiro Shimizu/ Shimizu Consulting
    - (New Leader) Tsuyoshi Nagashima/ Miraial
- The JEITA Silicon Wafer Technical Committee, which has collaborated with SEMI since 1981, was disbanded in 2013, and JEITA Standards will be abolished around 2015/03.
- Select JEITA/JEIDA standards will be transferred into SEMI.

Attachment: 1409_JA_SiW_LiaisonR_for_SEuropa_R1.0.ppt

4 Ballot Review

4.1 Document 5604, Line Item Revision to SEMI M1-0414 SPECIFICATIONS FOR POLISHED SINGLE CRYSTAL SILICON WAFERS and SEMI M20-1110 PRACTICE FOR ESTABLISHING A WAFER COORDINATE SYSTEM

Passed as approved

4.2 Document 5403, Withdrawal of SEMI MF534-0707, TEST METHOD FOR BOW OF SILICON WAFERS

Passed as balloted

4.3 Document 5702, Line Item Revision to SEMI M68-1109, PRACTICE FOR DETERMINING WAFER NEAR-EDGE GEOMETRY FROM A MEASURED HEIGHT DATA ARRAY USING A CURVATURE METRIC, ZDD

Passed with editorial changes

5 Old Business

None

6 New Business

6.1 Ballot authorization

5736: Line Item Revision to M41-1213 Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

Motion: To issue ballot 5736 in Cycle 7 for adjudication at SEMICON Japan.
By / 2nd: Tetsuya Nakai/Mike Goldstein
Discussion: None
Vote: 5-0

6.2 SNARF approval

Mike Goldstein presented a SNARF for New Standard: Specification Of Developmental 450mm Diameter Polished Single Crystal Notchless Silicon Wafers With Back Surface Fiducial Marks. The intent of this activity is to replace the existing notched wafer specification.

Motion: To approve the above SNARF
By / 2nd: Pinyen Lin/Mike Goldstein
Discussion: None
Vote: 8-0

7 Next Meeting and Adjournment

The next meeting of the EU Chapter of the Silicon Wafer Committee will be in October 2015 in Dresden, Germany, in conjunction with SEMICON Europa.

Minutes submitted by:
Andrea Busch