Japan Silicon Wafer Committee
Meeting Summary and Minutes

Japan Standards Summer Meetings 2013
June 7, 2013, 13:00 – 17:00
JPR Bldg. Conference Room1, SEMI Japan Office, Tokyo, Japan

Next Committee Meeting
September 3, 2013, 13:00-17:00 Japan Standard Time
Japan Standards Fall Meetings 2013, Tokyo, Japan

Committee Announcements (optional)
None

Table 1 Meeting Attendees

Co-Chairs: Naoyuki J. Kawai (The University of Tokyo), Tetsuya Nakai (SUMCO)
SEMI Staff: Hirofumi Kanno

Company	*Last*	*First*	*Company*	*Last*	*First*
The University of Tokyo	Kawai	Naoyuki	SUMCO	Kawai	Naoyuki
Consultant	Kumai	Sadao	Consultant	Takenaka	Takao
Self	Yoshise	Masanori	Kuroda Precision	Ito	Shinju
GlobalWafers Japan	Araki	Koji	Consultant	Shimizu	Yasuhiro
GlobalWafers Japan	Takeda	Ryuji	Hitachi Kokusai Electric	Matsuda	Mitsuhiro
Tokyo Electron	Mashiro	Supika	Renesas Electronics	Shiramizu	Yoshimi

Table 2 Leadership Changes

Group	*Previous Leader*	*New Leader*
International 450 mm Wafers Task Force (Japan Side)	Masaharu Watanabe (Semilab Japan)	Masaharu Watanabe (Semilab Japan) remains as a co-leader.
		Naoyuki J. Kawai (The University of Tokyo)

Table 3 Ballot Results (or move to Section 4, Ballot Review)

Document #	*Document Title*	*Committee Action*
--	Editorial Changes to SEMI M80-0812, Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 450 mm Wafers	**Passed**

Table 4 Authorized Ballots (or move to Section 7, New Business)

None

Table 5 Authorized Activities (or move to Section 7, New Business)

None

Note: SNARFs and TFOFs are available for review on the SEMI Web site at:
http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 6 New Action Items (or move to Section 8, Action Item Review)

Item #	*Assigned to*	*Details*
130607-1	Co-chairs of the Japan Silicon Wafer Committee	To confirm the organization structure of the International Advanced Surface Inspection Task Force (Japan Side) by SEMICON West
130607-2	Co-chairs of the Japan Silicon Wafer Committee	To ask Masaru Watanabe (Semilab Japan), who has currently been a co-leader of the International 450 mm Wafers Task Force, whether to continue the leadership position

Table 7 Previous Meeting Actions Items **(or move to Section 8, Action item Review)**

Item #	*Assigned to*	*Details*
130308-01	Naoyuki J. Kawai	Yasuhiro Shimizu had comments about withdrawal of the JEITA Standards EM-3501. Naoyuki J. Kawai informs the JEITA Silicon Technologies committee of his comments. **Done**
130308-02	Tetsuya Nakai	Tetsuya Nakai informs the GCS members of the transfer of JEITA Standards. **Done**
130308-03	SEMI Staff	SEMI Staff conducts the ballot action for Related Information in accordance with current SEMI Standards Regulations. **Done**
130308-04	Tetsuya Nakai	Tetsuya Nakai report what the local rule on the Global Silicon Wafer Committee should apply to the current revised SEMI Standards Regulation to the GCS members. **Done**
130308-05	Tetsuya Nakai	Tetsuya Nakai reports the committee decision about consideration of transfer of Related Information to the GCS members and give it in the liaison report at the next North America Spring meeting. **Done**

1 Welcome, Reminders, and Introductions

Naoyuki J. Kawia called the meeting to order at 13:00. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

2 Review of Previous Meeting Minutes

The committee reviewed the minutes of the previous meeting.

Motion: Approve the minutes of the previous meeting
By / 2nd: Tetsuya Nakai (SUMCO) / Takao Takenaka (Consultant)
Discussion: None
Vote: 10:0

Attachment: 01. Minutes for JA SiW Commitee130308_r2

3 Liaison Reports

3.1 *JRSC Report*

Naoyuki J. Kawai (The University of Tokyo) reported for the JRSC. Of note:

The next JRSC meeting and the Planning meeting are scheduled for August 31, 2013 at SEMI Japan office, Tokyo, Japan.

3.2 *Silicon Wafer GCS Report*

Tetsuya Nakai (SUMCO) reported for the Silicon Wafer GCS. Of note:

Doc. 5069, *Specification for 450 mm Wafer Shipping System* is currently on the Silicon Wafer and PIC joint GCS voting.

3.3 *North America Silicon Wafer Committee*

Hirofumi Kanno (SEMI) reported for the North America Silicon Wafer Committee. Of note:

- Meeting Information
- Committee Leadership Status
- Committee Organization Structure
- Ballot Results
  - Doc. 5450A, Revision to SEMI M49-0912, with Title Change to: Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations
    - Approved pending ISC A&R Review
  - Doc. 5559, New Auxiliary Information: Interlaboratory Evaluation Of Nondestructive Method For Measuring The Edge Contour Of Silicon Wafers
    - Approved pending ISC A&R Review
- New SNARFs
  - Int'l Polished Wafer TF
    - Doc. 5543, Line Items Revision to SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers
  - Int'l Annealed Wafer TF
    - Doc. 5583, Revision of SEMI M57-0413, Specifications for Silicon Annealed Wafers
- Workshop at SEMICON West
  - Silicon Wafers – Future Standardization to Enable the Transition
    - Since 2008, SEMI has published fifteen 450 mm wafer standards, guided by customer requirements and supplier feedback. These specifications, covering wafers, carriers, and loadports, have enabled the industry to continue the development of equipment, materials, interfaces, and processes, but further standardization will be necessary for a successful transition to manufacturing on 450mm wafers. Speakers from Intel, Samsung, and TSMC and others will introduce some of these new concepts during this seminar.
    - Proposals discussed during this workshop will be considered for standardization by the SEMI Standards Advanced Wafer Geometry Task Force under the Silicon Wafer Committee.
  - Wednesday, July 10, 2013 (2:30-5:30 PM), San Francisco Marriott Marquis
- Ballots Status for Cycle 4-2013
- Task Force Reports
- Staff Contact Information

Attachment: 02, NA Si Wafer Liaison Report 20130516

3.4 *Europe Silicon Wafer Committee*

Hirofumi Kanno (SEMI) reported for the Europe Silicon Wafer Committee. Of note:

- Silicon Wafer Committee Leadership Status and Meeting Inforamtion
- Task Forces with European Participation
- Task Force reports
- New Activities

Attachment: 03, EU Si Wafer liaison report March 2013

3.5 *JEITA Report*

Naoyuki J. Kawai gave the JEITA Report. Of note:

The JEITA Silicon Technology Committee was disbanded in March, 2013. JEITA members are considering the transfer of existing JEITA standards to SEMI Standards and Japan Society of Newer Materials. In future, SEMI Standards Silicon Wafer committee will need to have revision work of existing SEMI Standards in order to delete their descriptions for JEITA/JEITA Standards in reference Standards sections in the future.

3.6 JSPS Report

Takao Takenaka reported updates of the JSPS.

3.7 *SEMI Staff Report*

Hirofumi Kanno (SEMI) gave the SEMI Staff Report. Of note:

- Global SEMI Events
- Standards Meetings during SEMICON West
- Ballot Critical Dates
- Publication Update
- ISC A&R SC Summary February 2013
- Recent Regulations & Procedure Guide Revisions
- Contact Information

Attachment: 04, SEMI Staff Report 2013 June R0.1

4 Subcommittee & Task Force Reports

4.1 International Polished Wafers Task Force

Takao Takenaka (Consultant) reported for the International Polished Wafers Task Force.

Line items revision of SEMI M1 is on the voting in Cycle 4. There are some negatives for Line item 4.

4.2 International Epitaxial Wafers Task Force

Takao Takenaka reported for the International Epitaxial Wafers Task Force. The Task Force has been developing drafting doc. 5542, Line Item Revision to SEMI M62-0413, Specifications for Silicon Epitaxial Wafers

4.3 International Annealed Wafers Task Force

Koji Araki (GlobalWafers Japan) reported for the International Annealed Wafers Task Force. This report contained information on Doc.5583 (Revision to M57). The ballot is going to be adjudicated at SEMICON Japan.

4.4 International SOI Task Force

Tetsuya Nakai (SUMCO) reported for the International SOI Task Force. This report contained information on NA Spring meeting updates and Doc.5541 in Cycle4.

Attachment: 05, SOI TF Report_130607

4.5 Reclaim Wafer Task Force

No update

4.6 International terminology Task Force

There was no update for the International terminology Task Force.

The Japan Silicon Wafer committee asked the Japan Test Methods Task Force to reviews its related terminology and reports the result to the International Terminology Task Force. The action is taken care of by Ryuji Takeda (co-leader of the Japan Test Methods Task Force).

4.7 International Test Methods Task Force and Japan Test Methods Task Force

Ryuji Takeda gave their Task Force report.

GOI Activity: Doc.5030 (Revision of SEMI M60) is going to be adjudicated at SEMICON West.

Chemical Analysis Activity: Doc.4844B (*New Standard: Guide for the Measurement of Trace Metal Contamination on Silicon Wafer Surface by Inductively Coupled Plasma Mass Spectrometry*) has been developed. The document will be balloted in Cycle7.

Organic Analysis: the Task Force has been developing Doc.5389 (Revision to MF1982)

Heavy Metal Analysis: Doc.5313B (Revisions of SEMI MF1535) has been developed.

Attachment: 06, Test method TF Progress Report

4.8 International 450 mm Shipping Box Task Force

Yasuhiro Shimizu (Consultant) gave the Task Force activity report. Yasuhiro Shimizu propose the editorial changes to SEMI M80.

Motion: Approve the Editorial changes made to SEMI M80-0812, Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 450 mm Wafer:

Motion to revise Figure 17 and 18 of M80-0812 as an editorial change for the following reasons.

- Table 1 correctly shows the proper FP references for dimensions related to this feature.
- Figure 16 shows the correct FP callout relative to the feature and its related dimension.
- Figure 17 has an incorrect reference to BP, and the correct reference plane callout be FP, referring to dimension parameters in the figure
- Figure 18 does not contain any dimensional parameters.
- The text in section 13 describes the correct references to FP.

By / 2nd: Yasuhiro Shimizu (Consultant) / Sadao Kumai (Consultant)

Discussion: None

Vote: 10:0

Attachment: 07, Editorial Changes M80-0812

4.9 International 450 mm Wafer Task Force

Tetsuya Nakai reported an interest on 450 mm Notchless Wafer Standard was discussed by G450C.

Tetsuya Nakai recommended Naoyuki J. Kawai as a new co-leader of the International 450 mm Wafer Task Force.

Motion: Approve Naoyuki J. Kawai as a co-leader of the International 450 mm Wafer Task Force

By / 2nd: Tetsuya Nakai / SUMCO, Sadao Kumai / Consultant

Discussion: Discussed the number of co-leaders of Global Task Force based on PG 5.4.8.1,

Vote: 10:0

Action Item: Co-chairs of the Japan Silicon Wafer Committee to ask Masaru Watanabe (Semilab Japan), who has currently been a co-leader of the International 450 mm Wafers Task Force, whether to continue the leadership.

4.10 International Advanced Wafer Geometry Task Force and Japan AWG Task Force

Masanori Yoshise (self) gave the report.

- Ballot Review
  - Preview Doc 5430A – Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles
    - Ballot results of Cycle 1 2013: No reject
    - Adjudication at Semicon West 2013
  - Preview Doc 5450A- Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations
    - Ballot results of Cycle 1 2013; No reject, Comments from J Valley
    - Adjudication at SEMI NA Spring Meeting in April
- Ballot development
- Auxiliary Information Document on Geometry Parameters of SEMI M1. Peter Wagner reported document was developing. Will discuss at SEMICON West

Attachment: 08, AWG TF Report (1)

4.11 International Advanced Surface Inspection Task Force

No report.

Action Item: Co-chairs of the Japan Silicon Wafer Committee to confirm the organization structure of the International Advanced Surface Inspection Task Force (Japan Side) by SEMICON West.

5 Old Business

None

6 New Business

6.1 Standardization on 450 m Notch Free Wafer

Tetsuya Nakai (SUMCO) addressed Japan Silicon Wafer TC members and Japan Traceability TC members are going to have a joint meeting for standardization discussion on 450 mm notch free wafer.

7 Action Item Review

7.1 *Open Action Items*

None

7.2 *New Action Items*

Hirofumi Kanno (SEMI) reviewed the new action items. These can be found in the New Action Items table at the beginning of these minutes.

8 Next Meeting and Adjournment

The next meeting of the Japan Silicon Wafer committee is scheduled for September 3 at Japan Standards Fall Meetings 2013 in Toyo, Japan.

Respectfully submitted by:
Hirofumi Kanno
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Minutes approved by:

Naoyuki J. Kawai (The University of Tokyo), Co-chair	<Date approved>
Tetsuya Nakai (SUMCO), Co-chair	<Date approved>

Table 8 Index of Available Attachments [#1]

#	*Title*	#	*Title*
01	Minutes for JA SiW Commitee130308_r2	07	Editorial Changes M80-0812
02	NA Si Wafer Liaison Report 20130516	08	AWG TF Report(1)
03	EU Si Wafer liaison report March 2013		
04	SEMI Staff Report 2013 June R0.1		
05	SOI TF Report_130607		
06	Test method TF Progress Report		

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact [SEMI Staff Name] at the contact information above.