3D Packaging & Integration North America TC Chapter

Meeting Summary and Minutes

NA Standards Fall 2017 Meetings

Tuesday, November 7, 15:00 – 17:00

SEMI Headquarters, Milpitas, California

TC Chapter Announcements

Next TC Chapter Meeting

NA Standards Spring 2018 Meetings

Tuesday, April 10, 15:00 – 17:00

SEMI Headquarters, Milpitas, California

Table 1 Meeting Attendees

Italics indicate virtual participants

Co-Chairs: Richard Allen (NIST), Chris Moore (Frontier Semiconductor), Sesh Ramaswami (Applied Materials)
SEMI Staff: Laura Nguyen

Company	*Last*	*First*	*Company*	*Last*	*First*
Asahi Glass	Mikayama	Masaki	TEL	Tsuruta	Yota
Asahi Glass	Takahashi	Mark	TEL	Tsuyoshi	Mihara
BW & Associates	Wu	Bevan	TEL	Chu	Cristina
Corning	*Schmidt*	*Ilona*	Veeco	Lateef	Rezwan
Entegris	*Dennis*	*Jeff*	*Wispry*	*Hadizadeh*	*Rameen*
Intevac	Werbaneth	Paul			
mCube	*Bhandari*	*Sanjay*	SEMI	Amano	James
ProPrincipia	Draper	Don	SEMI	Nguyen	Laura
Sonoscan	Martell	Steve	SEMI	Shemansky	Frank

Table 2 Leadership Changes

WG/TF/SC/TC Name	*Previous Leader*	*New Leader*
Fan-Out Panel Level Packaging (FO-PLP) Panel TF (**new**)	None	Cristina Chu (TEL) Rich Allen (NIST)

Table 3 Committee Structure Changes

Previous WG/TF/SC Name	*New WG/TF/SC Name or Status Change*
None	Fan-Out Panel Level Packaging (FO-PLP) Panel TF (**new**)

Table 4 Ballot Results

None

Table 5 Activities Approved by the GCS between meetings of the TC Chapter

None

Table 6 Authorized Activities

Listing of all revised or new SNARF(s) approved by the Originating TC Chapter.

#	*Type*	*SC/TF/WG*	*Details*
-	TFOF	FO-PLP Panel TF	Fan-Out Panel Level Packaging (FO-PLP) Panel TF **(new)**

#1 SNARFs and TFOFs are available for review on the SEMI Web site at:
http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 7 Authorized Ballots

None

Table 8 SNARF(s) Granted a One-Year Extension

None

Table 9 SNARF(s) Abolished

None

Table 10 Standard(s) to receive Inactive Status

None

Table 11 New Action Items

None

Table 12 Previous Meeting Action Items

Item #	*Assigned to*	*Details*
2017July#01	Laura Nguyen, Rich Allen	Work with Cristina Chu to create survey, launch and have proposal/presentation at Fall meetings. Closed.
2017April#03	Rich Allen	To contact Victor Vartanian (pending) and David Read (no) to see if they are still interesting of being TF leader. Ongoing.

1 Welcome, Reminders, and Introductions

Rich Allen (NIST) was unable to be present to chair this meeting, he appointed Steve Martell (Sonoscan) to chair in his place.

Steve Martell (Sonoscan) called the meeting to order at 15:03. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

Attachment: SEMI Standards Required Meeting Elements

2 Review of Previous Meeting Minutes

The TC Chapter reviewed the minutes of the previous meeting.

Motion:	To accept the previous meeting minutes as written.
By / 2nd:	Cristina Chu (TEL) / Bevan Wu (BW&A)
Discussion:	None.
Vote:	8-0 in favor. Motion passed.

Attachment: [2017West3DS-IC Minutes FINAL

3 Liaison Reports

3.1 *3D Packaging & Integration Japan TC Chapter*

Laura Nguyen (SEMI) reported for the Japan TC Chapter. Of note:

Leadership

- Committee Co-chairs
  - To JRSC
    - 1st Chair person, Kazunori Kato (AiT)
    - 2nd Chair person, Haruo Shimamoto (AIST)
    - 3rd Chair person, Masahiro Tsuriya (iNEMI)
  - GCS
    - 1st GCS member, Kazunori Kato (AiT)
    - 2nd GCS member, Masahiro Tsuriya (iNEMI)Technical Architect

Current Organization Chart of Japan TC Chapter *{See attachment for Org Chart}*

Meeting Information

- Last meeting
  - Japan Fall 2017 Meetings (Wednesday, September 13, 2017, @SEMI Japan office, Tokyo)
- Next meeting
  - Japan Winter 2018 Meetings (Monday, February 5, 2018 @SEMI Japan office, Tokyo)

Document Review Summary at Japan Standards Summer 2017 Meetings

Doc #	Document Title	Committee Action
6148	Line Item Revision to SEMI G18-96 (Reapproved 0811) "Standard for Integrated Circuit Leadframe Material Used in the Production of Etched Leadframes" with non-conforming title change to "Specification for Integrated Circuit Leadframe Material Used in the Production of Etched Leadframes"	
Line Item 1	Change nonconforming title	Passed as balloted Superclean
Line Item 2	Change section titles to meet the requirement which is specified section 3.2 of Procedure Manual	Passed as balloted Superclean
6149	Line Item Revision to SEMI G38-0996 (Reapproved 0811) "Test Method for Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages"	
Line Item 1	Change section titles to meet the requirement which is specified section 3.2 of Procedure Manual	Passed as balloted Superclean
Line Item 2	Add "Calculation" section title and get re-formatted to meet the requirement which is specified section 3.2 of Procedure Manual	Passed as balloted Superclean
6150	Line Item Revision to SEMI G56-93 (Reapproved 0811) "Test Method for Measurement of Silver Plating Thickness"	

Line Item 1	Re-format some parts as to meet the requirement which is specified section 3.2 of Procedure Manual.	Passed as balloted Superclean
6151	Line Item Revision to SEMI G65-96 (Reapproved 0811) "Test Method for Evaluation of Leadframe Materials Used for L-Leaded (Gull Wing Type) Packages"	
Line Item 1	Re-format some parts as to meet the requirement which is specified section 3.2 of Procedure Manual.	Passed as balloted Superclean
6153	Reapproval of SEMI G90-0811: Specification for 300 mm Wafer Coin-Stack Type Shipping Container Used for Test and Packaging Processes	
6155	Line Item Revision to SEMI G62-95 (Reapproved 0811) "Test Method for Silver Plating Quality"	
Line Item 1	Re-format some parts as to meet the requirement which is specified section 3.2 of Procedure Manual.	Passed as balloted Superclean
6157	Reapproval of SEMI G23-0996 (Reapproved 0811): Test Method of Inductance for Internal Traces of Semiconductor Packages	Passed as balloted Superclean
6158	Reapproval of SEMI G42-0996 (Reapproved 0811): Specification for Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages	Passed as balloted Superclean
6159	Reapproval of SEMI G59-94 (Reapproved 0811): Test Method for Measurement of Ionic Contamination on Leadframe Interleafing and the Contamination Transferred from the Interleafing to the Leadframes	Passed as balloted Superclean
6160	Reapproval of SEMI G60-94 (Reapproved 0811): Test Method for the Measurement of Electrostatic Properties of Semiconductor Leadframe Interleafing Materials	Passed as balloted Superclean
6161	Reapproval of SEMI G66-96 (Reapproved 0811): Test Method for the Measurement of Water Absorption Characteristics for Semiconductor Plastic Molding Compounds	Passed as balloted
6162	Reapproval of SEMI G67-0996 (Reapproved 0811): Test Method for the Measurement of Particle Generation from Sheet Materials	Passed as balloted Superclean
6163	Reapproval of SEMI G68-0996 (Reapproved 0811): Test Method for Junction-to-Case Thermal Resistance Measurements in Air Environment for Semiconductor Packages	Passed as balloted Superclean
6164	Reapproval of SEMI G69-0996 (Reapproved 0811): Test Method for Measurement of Adhesive Strength Between Leadframes and Molding Compounds	Passed as balloted Superclean
6165	Reapproval of SEMI G71-0996 (Reapproved 0811): Specification for Barcode Marking of Intermediate Containers for Packaging Materials	Passed as balloted
6166	Reapproval of SEMI G89-0211: Specification for Leadframe Strip Size	Passed as balloted Superclean

*All those documents passed at A&R in August 2017.

SNARFs Approved at Japan Standards Summer 2017 Meetings

The following SNARFs were approved at the TC Chapter meeting held on July 24, 2017.

However, the TC Chapter agreed at the meeting held on September 13, 2017 that it will inactivate those Standards that have not been purchased or referenced even if the SNARFs for them were approved.

- Revision to SEMI G4-0302 (Reapproved 0811): Specification for Integrated Circuit Leadframe Materials Used in the Production of Stamped Leadframes
- Revision to SEMI G11-88 (Reapproved 0811): "Recommended Practice for RAM Follower Gel Time and Spiral Flow of Thermal Setting Molding Compounds" with non-conforming title change to "Practice for RAM Follower Gel Time and Spiral Flow of Thermal Setting Molding Compounds"
- Revision to SEMI G13-88 (Reapproved 0811): "Standard Test Method for Expansion Characteristics of Molding Compounds" with non-conforming title change to "Test Method for Expansion Characteristics of Molding Compounds"
- Revision to SEMI G15-93 (Reapproved 0811): "Standard Test Method for Differential Scanning Calorimetry of Molding Compounds" with non-conforming title change to "Test Method for Differential Scanning Calorimetry of Molding Compounds"
- Revision to SEMI G24-89 (Reapproved 0811): Test Method for Measuring the Lead-to-Lead and Loading Capacitance of Package Leads
- Revision to SEMI G25-89 (Reapproved 0811): Test Method for Measuring the Resistance of Package Leads
- Revision to SEMI G28-0997 (Reapproved 0811): Specification for Leadframes for Plastic Molded S.O. Packages

- Line Item Revision to SEMI G29-1296E (Reapproved 0811): Test Method for Trace Contaminants in Molding Compounds
- Revision to SEMI G43-87 (Reapproved 0811): Test Method for Junction-to-Case Thermal Resistance Measurements of Molded Plastic Packages
- Revision to SEMI G51-90 (Reapproved 0811): Specification for Plastic Molded (Metric) Quad Flat Pack Leadframes
- Revision to SEMI G55-93 (Reapproved 0811): Test Method for Measurement of Silver Plating Brightness

Task Force Updates

- Japan 450 mm Assembly & Test Die Preparation (ATDP) TF
  - The TFOF is not revised for the integration.
  - The TF has not been active for a year, but is not discharged.
- Thin Chip Handling TF
  - Before the integration, G97-0617: "SPECIFICATION FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING" is published.
  - The TFOF is not revised for the integration.
  - #5836: New Standard: Test Method for Adhesive Strength for Adhesive Tray Used for Thin Chip Handling
    - Ballot to be drafted
  - The TF is recruiting new members.
- Packaging Five Year Review TF
  - 16 documents passed at the TC Chapter meeting held on July 24, 2017
    - Details are shown in slide 6 through slide 9.
  - Those 16 documents passed at the A&R in August 2017.
    - Waiting for proofs
  - As mentioned in the slide 11, the TC Chapter agreed at the meeting held on September 13, 2017 that it will inactivate any of those legacy Packaging Standards that have not been purchased or referenced.
  - The decision will made for all those legacy Packaging Standards at the next TC Chapter meeting held on February 5, 2018
- Steering Group
  - Leadership: Masahiro Tsuriya/ iNEMI, Eiji Yoshino / Hitachi High-Technologies, Haruo Shimamoto / AIST
  - Below were listed at the meeting. Further discussion plans to be made to narrow down the work area.
    - Potential Areas:
      - PLP Panel Size (need more detail discussion for possibility)
      - Inspection/measurement Methodology on Delamination, Void, …
      - Measurement metrology of Mold resin parameters (Liquid, Granular, Sheet)
      - Keep-out or other design rules for dies placement
      - Dimension of outlet of direct imaging equipment

        - Fragility metrology for PLP/FOWLP device
        - Adhesion strength on molded surface Area
        - Handling, Transportation and Packing of molded panel (before singulation)
    - Next Meeting
        - Friday, December 15, 13:30-16:00
        - Conference Tower, Tokyo Big Sight
        - In conjunction with SEMICON Japan 2017
- Workshops for 3DS-IC Standardization before the integration
    - 1st Workshop
        - Held on Sept. 7, 2015 at SEMI Japan office
        - More than 60 attendees
        - Yole, ITRI, Tokyo Seimitsu and Toray Engineering made presentations
    - 2nd Workshop
        - Held on January 12, 2016 at SEMI Japan office
        - More than 60 attendees
        - Yole, Otsuka Electronics and Hitachi Chemical made presentations
    - 3rd Workshop
        - Held on June 6, 2016 at SEMI Japan office
        - More than 60 attendees
        - Fukuoka IST, Tohoku University and Toray Engineering made presentations
    - 4th Workshop
        - Held on June 19, 2017 at SEMI Japan office
        - More than 60 attendees
        - Toshiba, Hitachi Automotive Systems, PETRA made presentations

Staff Contact: Chie Yanagisawa, SEMI Japan (cyanagisawa@semi.org)

Attachment: 171025_JA_3DP&I_Liaison_v2_LN

3.2 *3D Packaging & Integration Taiwan TC Chapter*

Laura Nguyen (SEMI) reported for the Taiwan TC Chapter. Of note:

Leadership

- Committee cochairs: Wendy Chen (King Yuan Electronics), Roger Hwang (ASE), Chien-Chung Lin (ITRI)

Organization Chart *{See attachment for Figure}*

Meeting Information

- Previous meeting – 14:30-16:00, September 29, 2017, SEMI office, Hsinchu, Taiwan
- Next meeting – 14:30-16:00, January 9, 2018, SEMI office, Hsinchu, Taiwan

Task Force Updates

- Testing TF Report

  - New SNARF: "New Standard: Guide for Thin Chip Micro-Crack Inspection"
    - Draft Doc work in-progress
- Middle End Process TF Report
  - Doc. 5800 "New Standard: Guide for Wafer Edge Trimming for 3DS-IC Process"
    - Balloted in Voting Cycle 7-17
  - Study the feasibility of forming Fan-Out Task Force and contact potential companies:
    - Foundry: TSMC
    - Packaging: SPIL, ASE, PTI
    - PCB: Unimicron Technology Corp. (UTC)

Staff Contact: Dean Chang, SEMI Taiwan (dchang@semi.org)

Attachment: Taiwan 3D P &I Standards Committee Liaison Report_20171101

3.3 *SEMI Staff Report*

Laura Nguyen (SEMI) gave the SEMI Staff Report. Of note:

SEMI Global 2017 Calendar of Events

- SEMICON Europa (November 14-17, 2017; Munich, Germany)
- SEMICON Japan (December 13-15, 2017; Tokyo, Japan)

SEMI Global 2018 Calendar of Events

- SEMICON Korea (January 31-February 2; Seoul, Korea)
- 2018Flex/MSTC (February 12-15; Monterey, California)
- SEMICON China (March 14-16; Shanghai, China)
- SEMICON Southeast Asia (May 8-10; Kuala Lumpur, Malaysia)
- SEMICON West (July 10-12; San Francisco, California)

Upcoming North America Standards Meetings

- NA Standards Spring 2018 Meetings (April 9-12, 2018, SEMI HQ in Milpitas, California)
- SEMICON West 2018 (July 9-12, 2018, San Francisco, California)
- NA Standards Fall 2018 Meetings (November 5-8 [tentative], SEMI HQ in Milpitas, California)

Letter Ballot Critical Dates for 2017 & 2018

- Cycle 8-17: ballot submission due: Oct 13/Voting Period: Oct 27 – Nov 27
- Cycle 9-17: ballot submission due: Nov 16/Voting Period: Nov 29 – Dec 29
- Cycle 1-18: ballot submission due: Jan 3/Voting Period: Jan 16 – Feb 15
- Cycle 2-18: ballot submission due: Feb 7/Voting Period: Feb 20 – Mar 22
- Cycle 3-18: ballot submission due: Mar 9/Voting Period: Mar 23 – Apr 23
- Cycle 4-18: ballot submission due: Apr 20/Voting Period: Apr 30 – May 30

Critical Dates: http://www.semi.org/en/Standards/Ballots

Standards Publications Report

Cycle	*New*	*Revised*	*Reapproved*	*Withdrawn*
July 2017	0	1	1	0
August 2017	3	3	1	0
September 2017	0	1	3	0
October 2017	1	12	2	0

Total in portfolio – 978 (includes 210 Inactive Standards)

Nonconforming Titles (See PM Appendix 4) *{None}*

Five-Year Review

- SEMI 3D3-0613, Guide for Multiwafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames

SNARF 3 Year Status, TC Chapter may grant a one-year extension

- Doc. 5173: New Standard, Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack
    - SNARF was approved on 3/29/2011
    - One-year extension granted in Spring 2017
    - Action needed by Spring 2018

Attachment: [2017Fall] Staff Report 3DP&I

4 Ballot Review

NOTE 1: TC Chapter adjudication on ballots reviewed is detailed in the Audits & Review (A&R) Subcommittee Forms for procedural review. The A&R forms are available as attachments to these minutes. The attachment number for each balloted document is provided under each ballot review section below.

None

5 Subcommittee and Task Force Reports

5.1 *3DP&I Inspection and Metrology Task Force*

5.2 *3DP&I Bonded Wafer Stacks Task Force*

Steve Martell (Sonoscan) reported for both the 3DP&I Inspection and Metrology and 3DP&I Bonded Wafer Stacks Task Forces. Of note, during the task force meeting, the task force reviewed and continued working on the below draft documents. There is no new update at this time.

- 6175: New Standard, Guide on Measurements of Openings and Vias in Glass
- 6075: New Standard, Guide for Describing Glass-Based Material for Use in 3DS-IC Process

Please contact Ilona Schmidt (Ilona.schmidt@corning.com) and Rich Allen (richard.allen@nist.gov) if you would like to participate in these activites.

6 Old Business

6.1 *Previous Action Items*

Previous action items are noted in Table 12 in 'red' and for recent updates in 'blue'. There is no further old business.

7 New Business

7.1 *Fan-Out Panel Level Packaging Presentation and Survey Results*

Cristina Chu (TEL) addressed the committee on this topic.

Outline

- Rationale for FO-PLP Substrate Standardization
- Scope of FO-PLP Standardization Survey
- Results of FO-PLP Standardization Survey
- Conclusions
- Proposed next steps

Rationale for FO-PLP Substrate Standardization

- Rationale: FO-PLP needs substrate standard for HVM
  - Fan Out Wafer Level Packaging FO-WLP has entered HVM at 300 mm with Apple's production of the iPhone7 A10 Applications Processor
  - Processing fan out on panels could provide a cost savings vs wafers
  - *{see attachment for images}*
- Rationale: Tremendous cost advantage to panel vs wafer
  - Panel substrates today range from 300 – 920 mm on one size
  - Cost advantages depend on package and substrate size
  - Lack of standardization can provide a barrier to HVM
  - *{see attachment for images}*
- Rationale: Too much variation today in substrates for HVM
  - *{see attachment for images}*
- Rationale: A starting point for FO PLP adoption in HVM
  - Adoption of emerging technologies requires optimization across the entire production, not just one process *(even one bottleneck can critically slow down the adoption of a new technology)*
  - Equipment needs to fit in existing facilities
  - Equipment and material development ecosystem *(including lithography capability, chemistry consumption, photoresist usage and initial handling of warped panels)* is well established at 510 x 515 mm for many of the required processes
  - Propose spring boarding off of initial success where we've been able to validate the key manufacturing steps as a starting point to move this fan out technology to market at cost effective targets
  - Subsequent moves can be made to larger substrates once momentum has been establish
- Rationale: FO-PLP from LAB to FAB
  - FO-PLP requires workflow across various tools for
    - Loading panels
    - Picking and place die
    - Putting seed and resist on panels
    - Exposing panels

  - Plating panels

  … among many other processes

  - *{see attachment for images}*

Scope of FO-PLP Survey

- FO-PLP Survey: The SEMI Standards Questionnaire
  - To find answers about how relevant FO-PLP standardization is for the Semiconductor industry, direct stakeholders were invited to complete a simple questionnaire.
  - The survey was prepared by Tokyo Electron and Fraunhofer IZM and launched through the SEMI Standards organization.
  - The survey was launched in September 2017 and feedback was collected for approximately one month.

Survey Results

- Executive Summary
  - A good response was obtained from 63 survey participants, representing virtually every major player in the industry
    - Equipment Suppliers (~40%), Manufacturers & OSATS (~16%) , Materials Suppliers (16%), Institutions (4%)
  - Majority of the top substrate dimensions requested were
    - 510 x 515 mm
    - 600 x 600 mm
    - 300 x 300 mm

>70% of respondents are in favor of a SEMI standardization effort and >60% of respondents are willing to actively contribute to this effort

Proposed next steps

- Recommend initiation of a new task force
- TFOF is ready for review
- SNARF has been prepared and will be submitted for two-week TC Member review
- Tentative Time schedule:
  - TFOF approval November 2017
  - SNARF submission November 2017
  - 1st FO-PLP TF kick-off teleconference meeting November 2017
    - Tuesday, November 28, 11:00 AM EST (8:00 AM PDT, 5:00 PM CET)
    - Wednesday, November 29, 7:00 PM EST (8:00 AM China/Taiwan, 9:00 AM Tokyo, 4:00 PM PDT)
  - Creation of a first FO-PLP ballot (draft v.1): Dec 2017
  - Ballot authorization via GCS Dec 2017/Jan 2018
  - Ballot Voting Cycle 2-18 for adjudication at NA Spring meeting April 10, 2018

TFOF = Task Force Organization Form, SNARF = Standards New Activity Report Form

TF = Task Force, TC = Technical Committee

7.2 *New TFOF*

Cristina Chu (TEL) addressed the committee on this topic.

Motion: To approve new TFOF.
By / 2nd: Cristina Chu (TEL) / Mark Takahashi (Asahi Glass)
Discussion: None
Vote: 9-0 in favor. Motion passed.

Attachment: PanelSize-TFOF-November 2017 v5_LN

8 Next Meeting and Adjournment

The next meeting is scheduled for April 10 at the SEMI Standards North America Spring 2018 Meetings located at SEMI Headquarters in Milpitas, California. See http://www.semi.org/standards-events for the current list of events.

Tentative Schedule:

Tuesday, April 10

TBD 3DP&I Bonded Wafer Stacks (TF)

13:00-14:00 3DP&I Inspection and Metrology (TF)

14:00-15:00 FO-PLP Panel (TF)

15:00-17:00 3DP&I (C)

Adjournment: 16:07.

Respectfully submitted by:
Laura Nguyen
Coordinator, International Standards
SEMI Headquarters
Phone: 1.408.943.7019
Email: lnguyen@semi.org

Minutes tentatively approved by:

Steve Martell (Sonoscan), Bonded Wafer Stacks TF Leader	2/8/18
Richard Allen (NIST), Co-chair	<Date approved>
Sesh Ramaswami (Applied Materials), Co-chair	<Date approved>
Chris Moore (Frontier Semiconductor), Co-chair	<Date approved>

Table 13 Index of Available Attachments[#1]

Title	*Title*
SEMI Standards Required Meeting Elements	[2017Fall] Staff Report 3DP&I
[2017West] 3DS-IC Minutes FINAL	FO-PLP survey results_7 November Review 20171107
171025_JA_3DP&I_Liaison_v2_LN	PanelSize-TFOF-November 2017 v5_LN
Taiwan 3D P &I Standards Committee Liaison Report_20171101	

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Laura Nguyen at the contact information above.