3DS-IC North America TC Chapter

Meeting Summary and Minutes

SEMICON West 2017 Standards Meetings

Wednesday, July 12, 15:00 – 17:00

Marriott Marquis Hotel, San Francisco, California

TC Chapter Announcements

Next TC Chapter Meeting

NA Standards Fall Meetings 2017

Tuesday, November 7, 15:00 – 17:00

SEMI Headquarters, Milpitas, California

Table 1 Meeting Attendees

Italics indicate virtual participants

Co-Chairs: Richard Allen (NIST), Chris Moore (Frontier Semiconductor), Sesh Ramaswami (Applied Materials)
SEMI Staff: Laura Nguyen

Company	*Last*	*First*	*Company*	*Last*	*First*
Asahi Glass	Takahashi	Mark	NIST	Allen	Richard
Asahi Glass	Yoichiro	Sato	Solberg Technical Consulting	Solberg	Vern
BW & Associates / ITRI	Wu	Bevan	SuperSight	Perroots	Len
Cimetrix	Francis	David	Unily SC	Guillou	Yann
Flagship International Ltd.	Tuan	Andy T. F.	SEMI Japan	Yanagisawa	Chie
King Tuan Electronics Co., Ltd.	Chen	Wendy	SEMI Taiwan	Chang	Dean
Micron	Hacker	Jon	SEMI	Amano	James
NIST	Obeng	Yaw	SEMI	Nguyen	Laura

Table 2 Leadership Changes

None

Table 3 Committee Structure Changes

The proposal to transform the 3DS-IC and Assembly & Packaging Committees into a single, unified global technical committee (GTC) was approved at the International Standards Committee (ISC) meeting held on July 13, 2017 during SEMICON West.

Proposal Details:
To transform the 3DS-IC GTC and the Assembly & Packaging GTC into a unified GTC
To name the transformed GTCs as "3D Packaging and Integration" GTC
Each TC chapter of the unified GTC will inherit the co-chairs of the existing TC chapters

Previous WG/TF/SC Name (NA Chapter)	*New WG/TF/SC Name (NA Chapter)*
3DS-IC Bonded Wafer Stacks TF	3DP&I Bonded Wafer Stacks TF
3DS-IC Inspection and Metrology TF	3DP&I Inspection and Metrology TF

Table 4 Ballot Results

Document #	*Document Title*	*Committee Action*
5822A	New Standard, Specification for Reference Material for Bonded Wafer Stack Void Metrology	**Passed**, with editorial changes
6179	Reapproval of SEMI 3D1-0912, Terminology for Through Silicon via Geometrical Metrology	**Passed**, as balloted

#1 **Passed** ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.

#2 **Failed** ballots and line items were returned to the originating task forces for re-work and re-balloting or abandoning.

Table 5 Activities Approved by the GCS between meetings of the TC Chapter

None

Table 6 Authorized Activities

Listing of all revised or new SNARF(s) approved by the Originating TC Chapter.

None

#1 SNARFs and TFOFs are available for review on the SEMI Web site at:

http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 7 Authorized Ballots

None

Table 8 SNARF(s) Granted a One-Year Extension

None

Table 9 SNARF(s) Abolished

None

Table 10 Standard(s) to receive Inactive Status

None

Table 11 New Action Items

Item #	*Assigned to*	*Details*
2017July#01	Laura Nguyen, Rich Allen	Work with Cristina Chu to create survey, launch and have proposal/presentation at Fall meetings.

Table 12 Previous Meeting Action Items

Item #	*Assigned to*	*Details*
2017April#03	Rich Allen	To contact Victor Vartanian (pending) and David Read (no) to see if they are still interesting of being TF leader. Ongoing.
2017April#02	Junko Collins	To set up recurring meetings between NA and Japan every two weeks to discuss the details of the charter proposal and potentially have a final proposal to present at SEMICON West. CLOSED.

1 Welcome, Reminders, and Introductions

Richard Allen (NIST) called the meeting to order at 15:10. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

Attachment: SEMI Standards Required Meeting Elements

2 Review of Previous Meeting Minutes

The TC Chapter reviewed the minutes of the previous meeting.

Motion:	To accept the previous meeting minutes as written.
By / 2nd:	Steve Martell (Sonoscan) / Vern Solberg (Solberg Technical Consulting)
Discussion:	None.
Vote:	8-0 in favor. Motion passed.

Attachment: [2017Spring] 3DS-IC Minutes FINAL

3 Liaison Reports

3.1 *3DS-IC Japan TC Chapter*

Laura Nguyen (SEMI) reported for the 3DS-IC Japan TC Chapter. Of note:

- Committee Cochairs: Masahiro Tsuriya (iNEMI), Haruo Shimamoto (AIST)
- Organization Chart *{See attachment for Figure}*
- Meeting Information
    - Last meeting – Japan Summer 2017 Meetings: Monday, June 19, 2017 at SEMI Japan office, Tokyo
    - Next meeting – Japan Fall 2017 Meetings: Wednesday, September 13, 2017 at SEMI Japan office, Tokyo
- TF / SG Updates: Steering Group
    - Leadership: Masahiro Tsuriya/ iNEMI, Eiji Yoshino / Hitachi High-Technologies, Haruo Shimamot / AIST
- Charter
    - Define the work areas and review the global TC charter
    - Provide the following inputs and opportunities;
        - Plan technical workshop to promote the latest technologies and market trends on the 3DIC/SiP.
        - Brainstorm the areas of potential taskforce activities, and recommend the taskforce team formation to the Technical Committee
        - Handle any type of 3 dimensional IC package technologies including fan-out wafer level package or integrated SiP.
        - Provide the communication link from all layer of supply chain in Japan.
        - Interact with North America and Taiwan Technology Committee for the joint programs planning.
- Topics
    - Review the current charter as to expand the scope to cover the advanced package technologies (i.e. add FO-WLP), and plan to initiate discussion with other regional TC.
- Workshops for 3DS-IC Standardization

- 1st Workshop
  - Held on Sept. 7, 2015 at SEMI Japan office / More than 60 attendees
  - Yole, ITRI, Tokyo Seimitsu and Toray Engineering made presentations
- 2nd Workshop
  - Held on January 12, 2016 at SEMI Japan office / More than 60 attendees
  - Yole, Otsuka Electronics and Hitachi Chemical made presentations
- 3rd Workshop
  - Held on June 6, 2016 at SEMI Japan office / More than 60 attendees
  - Fukuoka IST, Tohoku University and Toray Engineering made presentations
- 4th Workshop
  - Held on June 19, 2017 at SEMI Japan office / More than 60 attendees
  - Toshiba, Hitachi Automotive Systems, PETRA made presentations

- Other 3DS-IC related activities in Japan
  - Thin Chip Handling Task Force under Assembly & Packaging Japan TC Chapter
    - New Standard: SPECIFICATION FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
      - Doc. 5835 was published as SEMI G97-0116 in January 2016
      - Ballot 6028 (Line Item Revision to SEMI G97-0116) was published as SEMI G97-0617 in June 2017.
  - Doc. 5836: New Standard: TEST METHOD FOR ADHESIVE STRENGTH FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
    - Ballot draft to be prepared
- Staff Contact: Chie Yanagisawa (cyanagisawa@semi.org)

Attachment: 170627_JA_3DS-IC_Liaison_v1

3.2 *3DS-IC Taiwan TC Chapter*

Laura Nguyen (SEMI) reported for the 3DS-IC Taiwan TC Chapter. Of note:

- Leadership
  - Committee cochairs: Wendy Chen (King Yuan Electronics), Roger Hwang (ASE), Chien-Chung Lin (ITRI)
- Organization Chart *{See attachment for Figure}*
- Meeting Information
  - Previous meeting – 14:20-15:30, June 29, 2017, SEMI office, Hsinchu, Taiwan
  - Next meeting – 14:30-16:00, September 29, 2017, SEMI office, Hsinchu, Taiwan
- 3DS-IC Standard Committee Highlights
  - Proposed SEMI 3DS-IC TC and Assembly & Packaging TC Integration to new TC name as "3D packaging and Integration TC".
  - The draft of Doc#5800 "New Standard: Guide for Wafer Edge Trimming for 3DS-IC Process" will be completed before next TC meeting.
  - Proposed to form the new TF " Fan-out TF" in the next TC

- Staff Contact: Dean Chang (dchang@semi.org)

Attachment: Taiwan 3DS-IC Standards Committee Liaison Report June 26 2017

3.3 *SEMI Staff Report*

Laura Nguyen (SEMI) gave the SEMI Staff Report. Of note:

- SEMI Global 2017 Calendar of Events
  - SEMICON West (July 11-13, 2017, San Francisco, California)
  - SEMICON Taiwan (September 13-15, 2017; Taipei, Taiwan)
  - PV Taiwan (October 12-14, 2017; Taipei, Taiwan)
  - SEMICON Europa (November 14-17, 2017; Munich, Germany)
  - SEMICON Japan (December 13-15, 2017; Tokyo, Japan)
- Upcoming North America Standards Meetings
  - NA Standards Fall 2017 Meetings (November 6-9 [tentative], SEMI HQ in Milpitas, California)
  - NA Standards Spring 2018 Meetings (April 2-5, 2018 [tentative], SEMI HQ in Milpitas, California)
  - SEMICON West 2018 (July 9-12, 2017, San Francisco, California)
- Letter Ballot Critical Dates for 2017
  - Fall 2017 adjudication
    - Cycle 6: ballot submission due: Jul 21/Voting Period: Aug 1 – Aug 31
    - Cycle 7: ballot submission due: Aug 18/Voting Period: Sep 1 – Oct 2

    Critical Dates 2017; http://www.semi.org/en/Standards/Ballots
- Standards Publications Report

Cycle	*New*	*Revised*	*Reapproved*	*Withdrawn*
March 2017	0	16	11	0
April 2017	0	6	0	0
May 2017	0	4	6	0
June 2017	2	4	0	0

Total in portfolio – 974 (includes 191 Inactive Standards)

- GTC Charter & Scope Review
  - Problem Statement
    - Majority of GTCs have defined charter but many don't have distinct Scope
    - It is stipulated in the Regulations that each GTC ought to have a distinct charter and scope. (See Regulations ¶5.7.3.2, §6.2)
      - As charter is often very generic (e.g., The XXXGTC discusses and creates consensus-based specifications and guides that promote mutual understanding and improved communication between users and suppliers of XXXX), it may not be useful to decide if the TF is within the scope of GTC or judge if a technical area proposal for installation of new GTC is really new.
  - Status as of today… *{See attachment for chart}*
    - SEMI Website publishes charter of GTC

- http://downloads.semi.org/web/wstdsbal.nsf/StdCharters

- Only a couple of GTCs clearly define scope while most of them define its Standards' scopes or at least include scope description in its charter.

- 3DS-IC GTC
- Current Charter
  - To explore, evaluate, discuss, and create consensus-based specifications, guidelines, and practices that, through voluntary compliance, will;
    - promote mutual understanding and improved communication between users and suppliers of 3DS-IC materials, carriers, equipment, automation systems and devices
    - enhance the manufacturing efficiency, capability and shorten 3DS-IC time-to-market
    - reduce manufacturing cost in the 3D-IC industry.
- Current Scope
  - Undefined
- Requirements/Process Reminders for TC Chapter Meetings
  - Standards Document Development Project Period
    - Project period shall not exceed 3 years (Regs 8.3.2)
      - SNARF approval to TC Chapter approval
    - If document development activity is found to be continuing, but cannot completed with the project period, TC Chapter may grant one-year extension at a time, as many times as necessary.
    - The TC Chapter should review the expiration dates for all applicable SNARFs at each TC Chapter meeting. (PM Note 10)
  - SNARF Review Period
    - A submitted SNARF for a new, or for a major revision to an existing, Standard or Safety Guideline is made available to all members of a TC Chapter's parent global technical committee for two weeks for their review and comment. (Regs 8.2.1)
      - If the SNARF is submitted at a TC Chapter meeting, the committee can review and approve, but the SNARF will need to be distributed for two weeks and then approved via GCS.
  - SNARF & TFOF Form: *{See attachment for forms}*
  - Procedures for Correcting Nonconforming Titles of Published Standards Document (PM Appendix 4)
    - Some Standards qualify for a special procedure where a line item change can be used to correct the titles. Otherwise, the corrective action will likely require a major revision.
    - Use of PIP form is allowed to correct title if all of the following conditions are met:
      - Standards having only one Subtype
      - Changes either Specifications to Specification or Test Methods to Test Method
      - No concomitant text change is required
      - Approved by at least one co-chair of the TC Chapter
      - Example:
      - SEMI F69-1213, Test Method~~s~~ for Transport and Shock Testing of Gas Delivery Systems
- Nonconforming Titles {*None*}

- Five-Year Review
    - Action by Spring 2018
        - SEMI 3D3-0613, Guide for Multiwafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames
- SNARF 3 Year Status, TC Chapter may grant a one-year extension
    - Doc. 5173: New Standard, Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack
        - SNARF was approved on 3/29/2011
        - One-year extension granted in Spring 2017
        - Action needed by Spring 2018

Attachment: [2017West] Staff Report 3DS-IC

4 Ballot Review

NOTE 1: TC Chapter adjudication on ballots reviewed is detailed in the Audits & Review (A&R) Subcommittee Forms for procedural review. The A&R forms are available as attachments to these minutes. The attachment number for each balloted document is provided under each ballot review section below.

4.1 Document # 5822A, New Standard, Specification for Reference Material for Bonded Wafer Stack Void Metrology

- The ballot passed TC Chapter review with editorial changes. See attachment for ballot adjudication.

Attachment: 5822AProceduralReview

4.2 Document # 6179, Reapproval of SEMI 3D1-0912, Terminology for Through Silicon via Geometrical Metrology

- The ballot passed TC Chapter review as balloted. See attachment for ballot adjudication.

Attachment: 6179Procedural Review

5 Subcommittee and Task Force Reports

5.1 *3DS-IC Inspection and Metrology Task Force*

Rich Allen (NIST) reported for this task force. This report contained information on ballot results, open SNARFs, IPC and JEDEC Liaison reports and brief discussion on the merger of the 3DS-IC GTC and Assembly and Packaging GTC.

- Ballot Review *{See section 4 of these minutes for Ballot results}*
    - Doc. 5822A, New Standard: Specification for Reference Material for Bonded Wafer Stack Void Metrology.
    - Doc 6179, reapproval of SEMI 3D1, TERMINOLOGY FOR THROUGH SILICON VIA GEOMETRICAL METROLOGY

See notes in ballot results document.

- Open SNARFs
    - Document 5976 – New Standard: Terminology for 3DS-IC Technology
    - Document 6175 – New Standard, Guide on Measurements of Openings and Vias in Glass

- Report from Activity leader Ilona Schmidt: Here I have to admit that not much progress was made. However, we found that we need to address an additional issue more importantly: It's about accuracy of the alignment, when we measure the coordinates of an array of TGVs on a panel or wafer.
- Here, we have started to work a test procedure, and we would have something to circulate or present for discussions fairly soon. The question is whether to incorporate this into 6175 or have a separate document. Or address this in the guide and have a test method extra? I also was wondering whether TSV would not have the same issue, but 3D5 seems not to address this issue at all.

- IPC Liaison report (IPC 7091)
  - This document, which is a general overall document on 3D, has been published.
- JEDEC Liaison report (JEP 158)
  - Currently being worked on in JEDEC as a revision
- Discussion on merger of 3DS-IC GTC and Assembly and Packaging GTC
  - Will review during TC Chapter meeting

Attachment: [Ballot Results] Cycle 04-17 3DS-IC_during meeting

Attachment: 2017-07 I&M Minutes

5.2 *3DS-IC Bonded Wafer Stacks Task Force*

Rich Allen (NIST) reported for this task force. This report contained information on opened SNARFs and a brief discussion on the topic about panel scale fan-out.

- Open SNARFs
  - Document 5173 – New Standard: Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack
  - Document 6075 – New Standard: Guide for Describing Glass-Based Material for Use in 3DS-IC Process *(former 5692)*
    - Report from Activity leader Ilona Schmidt: I will circulate this document the next weeks for comments to get approval to ballot at Fall meeting.
  - Document 6076 – New Standard: Specification for Identification and Marking for Bonded Wafer Stacks *(former 5174)*
- Discussion on Panel Scale Fan Out
  - Cristina Chu from TEL will be present during the TC Chapter meeting and present the problem statement.

Attachment: 2017-07 BWS Minutes

6 Old Business

6.1 *Previous Action Items*

Previous action items are noted in Table 12 in 'red' and for recent updates in 'blue'. There is no further old business.

7 New Business

7.1 *Panel Scale Fan Out Discussion*

Rich Allen (NIST) introduced Cristina Chu (TEL) who addressed the committee on this topic.

(Cristina Chu) I am part of Tokyo Electron; we are an equipment supplier, in the Boston area that builds tools that are focused on tools in advanced packaging. I am chair of the North East committee for SEMI in the Boston area and when I raised that to the members we have, they suggested I come to this meeting and share this concern.

Problem Statement (C.C.):

- A lot of interest from different customers for plating and sputtering tools for advanced packaging from the far back of the line.
- There are many different many sizes of wafers or other substrates that we either plate or sputter.
- Recently we've seen a lot of interest on plating or sputtering of panels, but we have seen a great deal of variation in the material itself and in the size of the material. So the sizes range from 400 mm x 500 mm to 600 mm x 600 mm.
- Much of the demand is for panels with dimensions in the range of 500, 510, and 515 mm.

Discussion:

(C.C) We've seen this for glass, epoxy, and a series of different substrate types, but there really has been a lack of standardization in terms of sizes of the substrate. A standardize substrate size would be extraordinarily useful.

(S.M.) I think we would have to start with certain size of the panel, don't think we can standardize materials but size we can.

(C.C.) That would be ideal.

(S.M.) Next thing we would look at is, does it fit within one of our task forces? Or would we have to create a new one? We'll have to put a survey out there and see what the industry leans toward. Start with a list of questions and go from there.

- Next steps: Cristina and Rich will work will Laura and James at SEMI to produce a survey and present results and possible TFOF at Fall 2017 meetings.

Action Item: 2017July#01, Laura and Rich to work with Cristina Chu to create survey, launch and have proposal/presentation at Fall 2017 meetings

7.2 *3DS-IC Charter Proposal Update*

Rich Allen (NIST) presented to the committee on this topic. Of note, contents of the presentation:

Transforming existing 3DS-IC GTC and Assembly & Packaging GTC into a unified GTC

Rationale

- As semiconductor packaging and integration technologies evolve, standards for these new technologies could fit into either the work area of 3DS-IC TC or the work area of the Assembly & Packaging TC. Emerging packaging technologies require 3D stacking IC technologies, including through-silicon via (TSV), as well as extended packaging technologies
- These new innovated semiconductor packaging technologies are difficult to clearly be categorized based on technology basis. This move cause overlapping the work areas among 3DS-IC TC and Assembly & Packaging TC
- One example is plans by both technical committees to expand their work area into: Fan-Out Wafer Level Packages

Current Charters of Assembly & Packaging GTC and 3DS-IC GTC *{please see attachment for details}*

Summary of Existing Global Technical Committees *{please see attachment for graph}*

- 3DS-IC
    - TC Chapters exist in North America, Japan, and Taiwan
    - Total membership: 117, Overlapping membership: 49
    - Japan TC chapter formed out of "Study Group"
    - The participating membership of this TC chapter is mostly comprised of the participating membership of the A&P TC Chapter
    - Number of existing current standards, 16 standards, all current
- Assembly and Packaging
    - TC Chapter only in Japan
    - Total membership: 103, Overlapping membership: 49
    - Number of existing standards
    - 97 standards, of which, Approximately 60 are current
    - Most of remainder are inactive, A few withdrawn

Common Interests of both Global Technical Committees

- Commonality of Members and Companies Participating on Both
    - 29 of common members
- Commonality of Technical Areas
    - Wafer Thinning & Handling
    - Wafer/Die Stacking and Interconnection Technology
    - Emerging packaging technologies, including Fan-Out Wafer Level Packaging and Panel Level Packaging
    - Packaging Media for Wafers (w/, w/o stacked) and chips (w/, w/o stacked)
- Current Overlap of Charter and Scope
    - Terminology of Advanced Packaging
    - Packaging Material, Packaging Equipment and Packing Materials

Proposal to transform existing 3DS-IC GTC and Assembly & Packaging GTC into a Unified GTC\

1. To transform the 3DS-IC GTC and the Assembly & Packaging GTC into a Unified GTC
2. To name the transformed GTCs as "3D Packaging and Integration" GTC
3. Each TC chapter of the unified GTC will inherit the co-chairs of the existing TC chapters

Proposed new Charter and Scope: 3D Packaging & Integration GTC

Charter

- To explore, evaluate, discuss, and create consensus-based specifications, guidelines, test methods, and practices that, through voluntary compliance, will:
- include the materials, piece parts, and interconnection schemes, and unique packaging assemblies that provide for the communication link between the semiconductor chip and the next level of integration, either single- or multi-chip configurations. It relates to the technologies for heterogeneous and other multi-chip packaging such as Fan-out/Fan-in Wafer Level Packaging, Panel Level Packaging, Three-Dimensional Stacking IC, device embedded packaging, flexible electronics technology

- promote mutual understanding and improved communication between users and suppliers, equipment, automation systems, devices, and services
- enhance the manufacturing efficiency, capability and shorten time-to-market and reduce manufacturing cost

Scope

- The 3D Packaging and Integration Committee develops standards for semiconductor devices, including processed wafers, chips, or multi-chip configurations to the next level of integration, either in single- or multi-chip configurations
- materials needed for 3D applications, including prime silicon and glass wafers, temporary and permanent bonding material, specifications needed for processed wafers and/or chips to enter an integration step, etc.
- the materials related to the elements of, interconnection schemes, and unique packaging assemblies that provide for the communication link between device and packaging
- the technologies for heterogeneous and other multi-chip packaging such as Fan-out/Fan-in Wafer Level Packaging, Panel Level Packaging, Three-Dimensional Stacking IC, device embedded packaging, and flexible electronics technology
- metrologies to support these 3D integration and packaging technologies

Attachment: Proposal of 3DS_AP Integration- rev.8a

7.3 *TEM Grid Survey Presentation*

Troy Morrison (Thermo Fisher Scientific) presented to the committee on this topic to see if this falls within the charter and scope to want to be included as an intercommittee ballot.

- Rationale: TEM metrology and analysis, from LAB to FAB
    - Semiconductor Industry metrology needs: TEM demand explodes to meet 3D transistor and multiple patterning challenges
    - Faster TEM data and more TEM data: TEM transition from Lab to Fab
    - ➔TEM microscopy needs to be fast, automated and easy to use
    - TEM microscopy requires a workflow with different tools to:
        - Prepare thin TEM lamellas from full wafers, Extract TEM lamellas from wafer, return wafers in manufacturing line, Measure TEM lamellas in TEM microscope
    - TEM lamellas are mounted on TEM "grids" and transported on these grids between the different tools: 300 mm FIB/SEM tool, TEM microscope and if needed, plasma cleaner, storage units,…
- Today's state-of-the-art in TEM metrology
    - Lamella preparation and extraction from full wafers is automated
    - Data acquisition (TEM imaging) and TEM metrology is automated
    - But TEM grid transport between tools is manual, using tweezers
        - Requires operator interventions, and has a non-zero failure rate…
        - Is slow and not really compatible with FAB operation…
    - A fully automated workflow requires automatic TEM grid handling
        - Like wafer handling, but unlike wafers, grids have different form-factors
- Why is standardization of TEM grids important?
    - Today the industry uses "3 mm grids" that have different form factors and do not respect a 'standard' for critical dimensions.

- There are several TEM grid suppliers (Ted Pella, Omniprobe, Agar,…)
- There are several TEM microscope suppliers (JEOL, Hitachi, FEI,..)
- Our customers need to be able to buy FIB/SEM and TEM systems from different suppliers (mix and match, best-in-class)
- ➔ compatibility between tools needs to be guaranteed
- ➔ a TEM grid should be compatible with all FIB/SEM/TEM systems

- How to standardize TEM grids?
  - A standard for diameter and thickness: to allow robotics for grid handling
    - Edge grippers (end effectors) of handling robots
    - Receptors of grids in TEM systems
  - A standard for the grid form factor: to ensure that all kind of receptors are compatible
    - A "cassette" for grid transport and grid storage
    - Mechanical positioning and alignment of grids in cassettes, or in TEM systems, plasma cleaners,…
  - A standard for grid material options: to control mechanical strength (deformation) and TEM performance (e.g. EDX spurious peaks)
  - A SEMI Standards task force in which IC manufacturers, TEM equipment and TEM grid suppliers define new standards together, enabling future developments of more automated TEM workflow solutions that are open rather than proprietary and industry-wide compatible/acceptable!
- Scope of TEM grid survey
- TEM grid survey: the SEMI Standards Questionnaire
  - To find answers about how relevant TEM grid standardization is for the Semiconductor industry, direct stakeholders were invited to complete a simple questionnaire.
  - The Survey was prepared by Thermo Fisher Scientific and launched through the SEMI Standards organization.
  - The Survey and questionnaire was launched on June 1, 2017 and feedback was collected for one month
  - The questionnaire was sent to various stakeholders:
    - IC manufacturers, SEMI Standard Program Members: PIC, Silicon Wafer, 3DS-IC
- Customer feedback survey results
- Executive Summary
  - A good response was obtained with all major IC manufacturers responding to the survey (n = 64)
  - 90% of current TEM sample handling is done manually and 75% of respondents would like to have it automated.
  - > 80% of respondents are in favor of having standard grids for:
    - Further automation (80%), TEM workflow efficiency (75%)
    - Compatibility between tools used in workflow (70%)
  - < 20% of respondents see drawbacks related to costs/compatibility
  - *> 80% of respondents are in favor of a SEMI standardization effort and 60% of respondents are willing to actively contribute to this effort*

Please see attachment for survey data.

After discussion, the committee agreed that the activity should be based in a different TC, but that there is likely enough interest that there should be liaison with the 3DS-IC Committee.

Attachment: TEM grid survey results_11JulyReview rev1

8 Next Meeting and Adjournment

The next meeting is scheduled for Tuesday, November 7, at the SEMI Standards North America Fall 2017 Meetings located at SEMI Headquarters in Milpitas, California.

See http://www.semi.org/standards-events for the current list of events.

Tentative Schedule:

Tuesday, November 7

13:00-14:00 3DP&I Inspection and Metrology (TF)

14:00-15:00 3DP&I Bonded Wafer Stacks (TF)

15:00-17:00 3DP&I (C)

Adjournment: 16:43.

Respectfully submitted by:

Laura Nguyen
International Standards Coordinator
SEMI Headquarters
Phone: 1.408.943.7019
Email: lnguyen@semi.org

Minutes tentatively approved by:

Richard Allen (NIST), Co-chair	October 11, 2017
Sesh Ramaswami (Applied Materials), Co-chair	<Date approved>
Chris Moore (Frontier Semiconductor), Co-chair	<Date approved>

Table 13 Index of Available Attachments[#1]

Title	*Title*
SEMI Standards Required Meeting Elements	6179ProceduralReview
[2017Spring] 3DS-IC Minutes FINAL	2017-07 BWS Minutes
170627_JA_3DS-IC_Liaison_v1	2017-07 I&M Minutes
Taiwan 3DS-IC Standards Committee Liaison Report June 26 2017	[Ballot Results] Cycle 04-17 3DS-IC_during meeting
[2017West] Staff Report 3DS-IC	Proposal of 3DS_AP Integration- rev.8a
5822AProceduralReview	TEM grid survey results_11JulyReview rev1

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Laura Nguyen at the contact information above.