NA Silicon Wafer Committee Meeting Minutes

SEMICON West 2013
Tuesday, 9 July, 2013, 1:00 PM - 5:00 PM
San Francisco Marriott Marquis, San Francisco, CA

Next Committee Meeting
October 29, 2013, SEMI HQ, San Jose, CA in conjunction with NA Fall Standards Meetings. Check www.semi.org/standards for latest update.

Attendees:

SEMI Staff
Kevin Nguyen – SEMI NA

Co-chair – Noel Poduje (Evergreen Enhancement)

Table 1 – Meeting Attendees

Last Name	*First Name*	*Company*
Bullis	Murray	Materials & Metrology*
Goldstein	Mike	Intel
Gupta	Dinesh	STA
Haller	Kurt	KLA-Tencor
Kathama	Hisashi	SUMCO
Kren	George	KLA-Tencor
Lee	KwangWook	G450C
Nakai	Tetsuya	SUMCO
Passek	Fritz	Siltronic
Perroots	Len	SuperSight
Sadaka	Mariam	SOITEC
Shimizu	Yasuhiro	Consultant*
Sinha	Jaydeep	KLA-Tencor
Sinton	Ron	Sinton Instruments
Sotirov	Zlatko	Genmark Automation
Staats	Christian	SHWITT
Valley	John	Sun Edison
Wagner	Peter	Self
Yoshise	Masanori	Yoshise Self

*Attended via teleconference

Table 2 – Leadership Changes

Group	*Previous Leader*	*New Leader*
Int'l Advanced Surface Inspection TF	George Kren (KLA-Tencor)	Kurt Haller (KLA-Tencor)
Int'l SOI TF	Mariam Sadaka (SOITEC)	Bich-Yen Nguyen (SOITEC)

Table 3 – Ballot Summary
Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

Document #	*Document Title*	*Committee Action*
5430A	Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles	Passed as superclean
5541	Revision of SEMI M41-0707, Specification of Silicon-on-Insulator (SOI) for Power Device/ICs	Passed as superclean

Document #	Document Title	Committee Action
5030	Revision to SEMI M60-0306, with title change to Test Method for Time Dependent Dielectric Breakdown Characteristics of Amorphous SiO2 Films for Silicon Wafer Evaluation	Passed as balloted
5543	Line Item Revisions to SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers	See below
Line Item 1	Correct the nanotopography entries	Passed as balloted
Line Item 2	Removal of apex length as an allowable specification for parameter-based edge profiles	Passed superclean
Line Item 3	Removal of Related Information 2 and all references thereto	Passed superclean
Line Item 4	Addition of reference to SEMI PV13 as a method for the measurement of carrier recombination lifetime and bulk iron content	Passed as balloted

Table 4 – Authorized Ballots

#	When	SC/TF/WG	Details
5583	Cycle 5-2013	Int'l Annealed Wafer TF	Revision of SEMI M57-0413, Guide for Specifying Silicon Annealed Wafers
5542	Cycle 5-2013	Int'l Epitaxial Wafer TF	Line Items Revision to SEMI M62-0413, Specifications for Silicon Epitaxial Wafers
5558	Cycle 6-2013	Int'l Test Methods TF	Revision of SEMI MF928-0305 (Reapproved 0211), Test Methods for Edge Contour of Circular Wafers and Rigid Disk Substrates(Re: To Include SEMI AUX)

Table 5 – Authorized Activities

#	Type	SC/TF/WG	Details
5604	SNARF	Int'l 450 mm Wafer TF	Revision to SEMI M1-0413, Specification for Polished Single Crystal Silicon Wafer (Re: Addition of Notchless 450 mm Wafers)
5605	SNARF	Int'l 450 mm Wafer TF	Line Item Revision to SEMI M1-0413, Specification for Polished Single Crystal Silicon Wafers (Re: Wafers for 16nm technology generation SFQR)
5606	SNARF	Int'l Test Methods TF	New Auxiliary Information: Interlaboratory Evaluation of Method 1 of SEMI MF673, Measuring Resistivity of Semiconductor Slices of Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage.
5607	SNARF	Int'l Test Methods TF	Revision of SEMI MF673-0305 (Reapproved 0611), Measuring Resistivity of Semiconductor Slices of Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

Note: SNARFs and TFOFs are available for review on the SEMI Web site at: http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 6 – Previous Meeting Actions Items

Item #	Assigned to	Details	Status
0413-1	Kevin Nguyen (SEMI Staff)	To email George Kren regarding SEMI M35-1107 Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection, which is due for 5 year review	Completed
0413-2	Kevin Nguyen (SEMI Staff)	To send JEITA round robin samples to Japan SEMI Staff for transferring to AIST	Completed

Table 7 – New Actions Items

Item #	Assigned to	Details
None		

1. Call to Order

Noel Poduje called the meeting to order and welcomed everyone who attended. A round of self introduction was made. All SEMI standards meetings are subjected to SEMI Anti-Trust Reminder and Guidelines concerning Patentable Technology. SEMI Regulations now require all attendees to be members of SEMI standards. Membership enrollment is at www.semi.org/standardsmembership. Agenda was reviewed and proceed.

2. Review of Schedule for the Next Meeting (NA Fall Meetings, Oct 28-29, 2013)

The next meeting is tentatively scheduled at the SEMI HQ on October 28-29, 2013 in San Jose, CA in conjunction with NA Fall Standards Meetings. Check www.semi.org/standards on the calendar of entry for the latest schedule and meeting location. Tentative schedule for the next meeting is as follows:

Monday, Oct 28, 2013

Int'l SOI (TF) 08:30-09:30	Int'l Annealed Wafer/ Epitaxial Wafer (TFs) 09:30-10:30	Int'l Test Methods (TF) 10:30-11:30	Int'l Terminology (TF) 11:30-12:00	Int'l Advanced Surface Inspection (TF) 13:00-14:00	Int'l Advanced Wafer Geometry (TF) 14:00-17:30

Tuesday, Oct 29, 2013

Int'l Polished Wafer (TF) 08:30-10:00	Int'l 450 mm Wafer (TF) 10:00-12:00	Silicon Wafer (C) 13:00-17:00	

3. Review and Approval of the Minutes from NA Spring meetings, April 2, 2013 in Santa Clara, CA

The meeting minutes reviewed. No change was made.

Motion: Accept the minutes of the previous meeting as submitted
By / 2nd: Dinesh Gupta (STA)/Len Perroots (Super Sight)
Discussion: None
Vote: Unanimous. Motion passed

Attachment – 1, Minutes NA SiWfr 20130402

4. Liaison Reports

4.1. GCS

Noel Poduje reported the meeting minutes for the GCS. For future meeting, Noel requested the GCS meeting room to be placed in a separate room, not the same with other TF since these meetings do not always end on time.

The followings were reported:

- Wafer specifications in documents (e.g., M1, M57, etc.) should be in appendix and not related information so it cannot be changed without ballot.
- Clarification of procedure for SNARF submission and ballot voting – It is appropriate to approve both SNARF and ballot if consensus was achieved in the TF.
- Line items – Whether a line item is a "major change" must be decided by the committee. If it is, then the whole document must be balloted.
- GCS vote

- If there are 6 members of the GCS but only 5 votes and the vote is 3-2 is this a majority? Not clear yet.

Attachment – 2, GCS130708

4.2. Europe Committee

Report was given by Peter Wagner. Highlights.

- Last Meeting
  - October 9-11, 2012 in conjunction with SEMICON Europa, Dresden, Germany
- Next Meeting
  - October, 2013 in conjunction with SEMICON Europa, Dresden, Germany
  - Check www.semi.org/standards calendar of event for latest update
- EU Silicon Wafer Committee
  - New Leader (Friedrich Passek (Siltronic))
- Int. Advanced Wafer Geometry TF
  - Meeting Berlin on March 13, 2013
  - Doc 5430A, Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles: passed ballot without negatives or comments
  - Revisions of SEMI M1 on-going
  - New auxiliary document illustrating flatness metrics under development
- Int. Polished Wafer TF
  - Meeting in Berlin, March 13, 2013
  - New draft document under development: Specification for Polished Single Crystal Silicon Wafers for GaN-on-Silicon Applications
- Int. Test Methods TF
  - No meeting in Europe for a while
  - Interaction with Japanese and NA TFs regarding
    - Doc 4846C, Revision to MF1982,Test method for Analyzing Organic Contaminants on Silicon Wafer Surface by Thermal Desorption Gas Chromatography, and
    - Doc 4844B, Guide for the measurement of trace metal contamination on silicon wafer surface by inductively coupled plasma mass spectrometry
    - Doc 5313C, Revision to MF1535, µPCD measurement

Attachment – 3, EU Si Wafer liaison report_March 2013

4.3. Japan Committee

Tetsuya Nakai (SUMCO) reported. Highlights.

- Last Meeting
  - June 7, 2013 at SEMI Japan, Tokyo
- Next Meeting
  - September 3, 2013 at SEMI Japan, Tokyo
- Ballots resulted from last meeting
  - Editorial changes made to SEMI M80-0812, Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 450 mm Wafers
- All other task forces are international and are collaborating with NA and Europe.
- Japan Test Method Task Force
  - Drafting
    - Doc. 5389, Revision to SEMI MF1982, Test method for analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography
    - Doc. 4844B, New Standard: Guide for the Measurement of Trace Metal Contamination on Silicon Wafer Surface by Inductively Coupled Plasma Mass Spectrometry.

Attachment: 4, JP_SiW_NA SW_R0.1

5. Staff Report

Report was given by Kevin Nguyen. Highlights:

- 2013 & 2014 Event

Event Name	*Event Details*
SOLARCON India	**August 1-3, 2013** **Bangalore**
SEMICON Taiwan **LED Taiwan**	**September 4-6, 2013** **Taipei**
SEMICON Europa	**October 8-10, 2013** **Dresden, Germany**
PE2013 – Plastic Electronics Exhibition and Conference	**October 8-10, 2013** **Dresden, Germany**
PV Taiwan	**October 30 – November 1, 2013** **Taipei**
SEMICON Japan	**December 4-6, 2013** **Chiba**
SEMICON Korea	**February 12-14, 2014** **Seoul**
LED Korea	**February 12-14, 2014** **Seoul**

- Silicon Wafers – Future Standardization to Enable the Transition (2:30 PM to 6:00 PM)
  - Agenda:
    - Towards 450 mm Silicon Wafers, Mike Goldstein (Intel)
    - Notchless Wafer, Pinyen Lin (G450C)
    - New Edge Exclusion Proposal, Kwangwook Lee (G450C)
    - Wafer Geometry for Advanced Nodes, Gerd Pfeiffer (IBM)
    - Challenges during 450 mm Silicon Processing, Hisashi Furuya (SUMCO)
    - 450 mm Facilities Planning, Allen Ware (F450C)
    - G450C Component Lift Program Update, Les Marshall (G450C)
  - Proceedings are available at https://sites.google.com/a/semi.org/siwaferfuturestandardstransition/

- NA Standards Fall 2013 Meetings
  - October 28-31
  - SEMI Headquarters in San Jose, California
  - Inviting local companies willing and able to host some of the meetings to maintain one-week format.
- Technical Ballot Critical Dates
  - Cycle 5, 2013
    - Ballot Submission Date: July 18
    - Voting Period Starts: July 29
    - Voting Period Ends: August 29
  - Cycle 6, 2013
    - Ballot Submission Date: August 15
    - Voting Period Starts: August 29

    - Voting Period Ends: September 30
- June 2013 Cycle Publication Cycle
    - New Standards: 10
    - Revised Standards: 2
    - Reapproved Standards: 4
    - Withdrawn Standards: 0
- Total SEMI Standards in portfolio: 887
    - Includes 94 Inactive Standards

Attachment – 5, SEMI Staff Report (West 2013)

6.0 Ballot Review

6.1 Document 5430A, Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles

6.1.1 Document passed technical review as balloted and was forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 6, 5430AProceduralReview

6.2 Document 5541, Revision of SEMI M41-0707, Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

6.2.1 Document passed technical review as balloted and was forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 7, 5541ProceduralReview

6.3 Document 5543, Line Item Revisions to SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers

- Line Item 1 - Correct the nanotopography entries
- Line Item 2 - Removal of apex length as an allowable specification for parameter-based edge profiles
- Line Item 3 - Removal of Related Information 2 and all references thereto
- Line Item 4 - Addition of reference to SEMI PV13 as a method for the measurement of carrier recombination lifetime and bulk iron content

6.3.1 All line items passed technical review as balloted and were forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 8, 5543ProceduralReview

6.4 Document 5030, Revision to SEMI M60-0306, Test Method for Time Dependent Dielectric Breakdown Characteristics of SiO2 Films for Si Wafer Evaluation with title change to Test Method for Time Dependent Dielectric Breakdown Characteristics of Amorphous SiO2 Films for Silicon Wafer Evaluation

6.4.1 Document passed technical review as balloted and was forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 9, 5030ProceduralReview

7.0 Task Force Reports

7.1 Specifications Group

7.1.1 Int'l 450 mm Wafer TF/Mike Goldstein (Intel)

Mike Goldstein reported.

- The notchless program was reviewed. Pinyen Lin (G450C) presented an update of the consortium activities. Nakai-san presented an update of the notchless wafers activities in Japan.
- The edge exclusion program was also reviewed. Kay Lee (G450C) presented an update of the consortium activities.

Mike presented the SNARF for an activity for Notchless 450 mm Wafers Specification.

Motion: To approve a SNARF, Revision to SEMI M1-0413, Specification for Polished Single Crystal Silicon Wafer (Re: Addition of Notchless 450 mm Wafers)
By / 2nd: Dinesh Gupta (STA)/Mike Goldstein (Intel)
Discussion: The SNARF was approved in the task force as a separate document. However, after discussing in the committee, it would be appropriate to revise SEMI M1 instead.

In reviewing the SNARF, John Valley (Sun Edison) informed the committee that there is a published patent "Production of Notchless Wafer (publication number US5993292 A)". It was informed to the committee.

According to Mike Goldstein (Intel), there are number of ways of producing notchless wafer. The referenced patent is one of the methods, not THE only method of producing notchless wafer.

Pinyen Lin (G450C), the main driver for the 450 mm notches wafer standard, is aware of the patent.

In moving forward, it is the best to the knowledge of the NA Silicon Wafer committee, the use of patented technology or a copyrighted item(s) is NOT required for the activity in question. Also, it was assumed that the activity being proposed by G450C will not be required the use of patented technology.

Vote: 13/0 in favor of approving the SNARF. Motion passed

For meeting minutes, please see attachment.

Attachment – 10, Notchless SNARF rev1
Attachment – 11, SEMI 450mm Si wafer TF 2013

7.1.2 Int'l Epitaxial Wafer TF/ Dinesh Gupta (STA)

Dinesh reported doc. 5542, Line Items Revision to SEMI M62-0413, Specifications for Silicon Epitaxial Wafers, which is ready for cycle 5-2013 ballot submission.

Motion: To authorize doc. 5542 for cycle 5-2013 for adjudication at SEMICON Japan
By / 2nd: Dinesh Gupta (STA)/Jaydeep Sinha (KLA-Tencor)
Discussion: None
Vote: Unanimous. Motion passed

Attachment – 12, MinEpiTF0713

7.1.3 Int'l Annealed Wafer TF/Dinesh Gupta (STA)

Dinesh Gupta reported doc. 5583, Line Items Revision to SEMI M57-0413, Specifications for Silicon Annealed Wafers, is also ready for cycle 5 ballot.

Motion: To send doc. 5583 for cycle 5-2013 for review at SEMICON Japan
By / 2nd: Dinesh Gupta (STA)/Tetsuya Nakai (SUMCO)
Discussion: None
Vote: Unanimous. Motion passed

Attachment – 13, MinAWiMtg0713

7.1.4 Int'l SOI TF/Mariam Sadaka (SOITEC USA)

Mariam Sadaka reported.

- Ballot Doc. 5541, Revision of SEMI M41-0707 Specification of Silicon-on-Insulator (SOI) for Power Device/ICs, was approved by committee.
- New Business: Action Items
  - Photonics: Ask if Opsis is willing to present & discuss specs in the next meeting
  - MEMS: Discuss with the MEMS TF leader how we can collaborate/help
  - High Resistivity SOI: Start discussion around building a new spec
  - 3D-IC: understand the needs & application of SOI
- Mariam stated that her responsibilities at SOITEC have shifted. Thus, she would like to step down from the task force after chairing for over a year. Mariam also would like to nominate her colleague, Bich-Yen Nguyen, as a successor.

Motion: Approve Bich-Yen as the co-chair of the SOI Task Force
By / 2nd: Dinesh Gupta (STA)/Tetsuya Nakai (SUMCO)
Discussion: Mariam will still attend future meetings to bring Bich-Yen to speed. On behalf of the NA Silicon Wafer committee, Noel expressed appreciation Mariam for an outstanding job and dedication in the task force.
Vote: Unanimous. Motion passed

Attachment – 14, NA SOI TF-REPORTING-Jul 8-2013

7.1.5 Int'l Polished Wafer TF/Murray Bullis (Materials & Metrology)

Murray reported.
Document 5543, Revisions to SEMI M1-0413 Specifications for Polished Single Crystal Silicon Wafers, passed committee review. In addition, the followings were discussed in the meeting.

- Changes are needed for SEMI draft document 5500 on Silicon Wafers for Gallium Nitride on Silicon applications.
- Consideration of reduction of specified edge exclusion of 450 mm wafers by 0.5 mm was discussed by Kay Lee (G450C). This topic will be further discussed at the next meeting.

Attachment – 15, Minutes of International Polished Wafer Task Force

7.2 Metrology Group

7.2.1 Int'l Advanced Wafer Geometry TF/Jaydeep Sinha (KLA-Tencor)

Minutes were presented by Jaydeep Sinha. Highlights:

Two presentations were made.

1. NT and ZDD scaling for Reference wafers: Dieter Mueller presented the need for NT scaling and brought up the limitations of current NT definition in SEMI M78. Filter size needs adjustment to remove lower order shape component fed through 20X1 filter size. Also litho Non-correctable errors driving the need to defining the analysis area similar to Litho field with peak to valley type of metric output. Dieter has submitted a SNARF to drive this definition change.

2. Edge exclusion proposal G450C: by KwangWook Lee, G450C. Mr. Lee had a proposal to extent FQA radius by another 0.5 mm (from 223 mm radius to 223.5 mm radius). This was primarily driven by Yield. A SNARF will be brought at the Polished Wafer task force and will be added to AWG to incorporate in M49.

New Business

1. Revision of M78, Adjustment for NT filter size and changes FQA for ZDD computation.

SNARF was presented, but this proposal will require the use of patented technology. Current version M78, Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing, is not required for the use of patent. On the contrary, this new proposed SNARF suggests there is no alternative to the use of patented technology or copyrighted item. Fritz Passek recommended this proposal to be postponed. The SNARF was dropped. No voting took place.

2. Aligning ITRS with AWG regarding proposed values. It was reported that Mike mentioned that for 450 mm wafers the nominal expectations for geometry parameters are pulled back (relaxed) compared to ITRS. 450mm wafer 16nm generation SFQR was defined based on ITRS technology node value. However because of the divergence between DRAM and Logic road maps we have an anomaly low value. It is suggested to use lithography requirements to adjust the SFQR values

A New SNARF for Line Item Revision to SEMI M1-0413, Specification for Polished Single Crystal Silicon Wafers (Re: Wafers for 16nm technology generation SFQR) was proposed.

Motion: To approve Line Item revision to M1 SNARF
By / 2nd: Mike Goldstein (Intel)/Fritz Passek (Siltronic)
Discussion: None
Vote: Unanimous. Motion passed

3. SEMI M1 Metric Illustration: Peter went through a developmental document illustrating definitions of the geometry metrics. Auxiliary document development still in progress. Update will be provided at SEMI Europa in October 2013.
4. Doc. 5503 revision to MF1390 to add bow measurement
5. Noel brought up the need to define Bow in SEMI standard. Bow Standard MF534 seemed to be impractical for automated measurement and does not adequately define bow. His proposed additions did not change data acquisition or data processing and provided a methodology to calculate Bow. Members in the task force agreed with Noel's proposal. Further discussion will be held at the next meeting.

For complete AWG meeting minutes and all other materials, please refer to attachments below.

Attachment -16, SFQR update SNARFev1
Attachment -17, AWG TF July 2013

7.2.2 Int'l Advanced Surface Inspection TF/George Kren (KLA-Tencor)

George Kren discussed an old business with doc. 5503, line item revision to M52-0912 Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm to 11 nm Technology Generations. Further modidification is needed on table 1, line 1.13 on Particulate Contamination row. The revised SNARF was presented.

Motion: To approve revised SNARF for doc. 5503
By / 2nd: George Kren (KLA-Tencor)/Dinesh Gupta (STA)
Discussion: None
Vote: Unanimous. Motion passed

A new leader for the ASI task force has been identified. Kurt Haller (KLA-Tencor) was nominated to be the co-leader of NA ASI Task Force.

Motion: To endorse Kurt Haller (KLA-Tencor) as the co-leader of the ASI TF
By / 2nd: George Kren (KLA-Tencor)/Peter Wagner (Self)
Discussion: None
Vote: Unanimous. Motion passed

Lastly, a presentation by Joann Qiu (Intel) on ASI roadmap was made in the task force. See below for the presentation.

Attachment -18, M52 SNARF
Attachment -19, Thoughts on ASI Roamap - SEMI ASI TF July 8, 2013

7.3 Committee Task Forces

7.3.1 Int'l Test Methods TF/Dinesh Gupta (STA)

Dinesh reported document 5030, Revision to SEMI M60-0306, Test Method for Time Dependent Dielectric Breakdown Characteristics of SiO2 Films for Si Wafer Evaluation with title change to Test Method for Time Dependent Dielectric Breakdown Characteristics of Amorphous SiO2 Films for Silicon Wafer Evaluation, passed committee review. A future revision is needed to deal with a comment submitted by Nakai-san.

Murray Bullis also reported doc. 5559, New Auxiliary Information: Interlaboratory Evaluation Of Nondestructive Method For Measuring The Edge Contour Of Silicon Wafers, which was approved at the last meeting, is not published yet. As soon as it is published, a revision of SEMI MF928 will be issued immediately in either cycle 5 or 6 to include the auxiliary inofmration.

Interlaboratory Evaluation of Method 1 of SEMI MF673, Measuring Resistivity of Semiconductor Slices of Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage.

- When the standard MF673 was transferred to SEMI in 2002, this research report was apparently not included in the material transferred. Early this year, there was an inquiry concerning this report. A copy was found in the files maintained by several of the volunteer members of the program and this is now being prepared as a SEMI AUX publication.

  Motion: To approve the SNARF
  By / 2nd: Dinesh Gupta (STA)/Tetsuya Nakai (SUMCO)
  Discussion: None
  Vote: Unanimous. Motion passed

- A SNARF for Revision of SEMI MF673-0305 (Reapproved 0611), Measuring Resistivity of Semiconductor Slices of Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage, was also submitted.

  Motion: To approve the SNARF
  By / 2nd: Dinesh Gupta (STA)/Tetsuya Nakai (SUMCO)
  Discussion: None
  Vote: Unanimous. Motion passed

- There was a brief discussion on MF1535 and lifetime, in general. See attachment below for submitted reports

Attachment -20, SNARF MF673 RR

Attachment -21, SNARF MF673 July 2013
Attachment -22, MinTestMethodsMtg0713
Attachment -23, TestMethodsAttachmentsJuly2013

7.3.2 Int'l Terminology TF/Murray Bullis (Materials and Metrology)

Murray reported the terms for Polysilicon, Wafer packaging, Microscopy and optics will be developed at this time.
For New Business,

- Lifetime Terminology review to discuss correction of the following definitions in SEMI M59: 1/e lifetime, bulk recombination lifetime and recombination lifetime, and add a definition for carrier recombination lifetime. These definitions are needed for the proposed revision to SEMI MF1535-0707 (Document 5313C) and will be discussed in details at the meeting.

Attachment -24, Minutes of International Terminology Task Force

8.0 Old Business

5 Year Review. The following document is overdue for 5 year review.

- SEMI M35-1107, Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection
  - M35 should be reviewed by the Int'l ASI TF.

9.0 New Business

None

10.0 Action Item Reviews

Kevin Nguyen reviewed the old action items. There were two new actions items at this meeting noted in **table 7**.

11.0 Adjourn

The meeting was adjourned at 5:00 PM.
These minutes are respectfully submitted by:

Kevin Nguyen,
SEMI NA Standards Committee Manager
Phone: 408-943-7997
Email: knguyen@semi.org

Minutes approved by:
Noel Poduje (SMS) – Co-chair Date:
Dinesh Gupta (STA) – Co-chair Date:

Table 8 – Index of Attachment Summary

#	*Title*	#	*Title*
1	Minutes NA SiWfr 20130402	13	MinAWiMtg0713
2	GCS130708	14	NA SOI TF-REPORTING-Jul 8-2013
3	EU Si Wafer liaison report_March 2013	15	Minutes of International Polished Wafer Task Force
4	JP_SiW_NA SW_R0.1	16	SFQR update SNARFev1
5	SEMI Staff Report (West 2013)	17	AWG TF July 2013
6	5430AProceduralReview	18	M52 SNARF
7	5541ProceduralReview	19	Thoughts on ASI Roamap - SEMI ASI TF July 8, 2013
8	5543ProceduralReview	20	SNARF MF673 RR
9	5030ProceduralReview	21	SNARF MF673 July 2013
10	Notchless SNARF rev1	22	MinTestMethodsMtg0713
11	SEMI 450mm Si wafer TF 2013	23	TestMethodsAttachmentsJuly2013
12	MinEpiTF0713	24	Minutes of International Terminology Task Force

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Kevin Nguyen at the contact information above