Silicon Wafer NA TC Chapter
Meeting Summary and Minutes

SEMICON West

Tuesday, July 11, 2017

1:00 PM – 5:00 PM

San Francisco Marriott Marquis, San Francisco, California

TC Chapter Announcements

Next TC Chapter Meeting
Tuesday, April 10, 2018 Milpitas, CA in conjunction with the NA Spring Standards Meeting 2018. Check www.semi.org/en/standards for the latest update.

Table 1 Meeting Attendees

Co-Chairs: Dinesh Gupta (STA), Noel Poduje (SMS)
SEMI Staff: Kevin Nguyen (SEMI HQ), Dean Chang (SEMI Taiwan), Junko Collins (SEMI Japan)

Company	*Last*	*First*	*Company*	*Last*	*First*
NIST	Allen	Rich	Thermo Fisher Scientific	Morrison	Troy
STA	Gupta	Dinesh	SUMCO	Nakai	Tetsuya
KLA-Tencor	Haller	Kurt	Siltronic	Passek	Fritz
Hitachi High Tech	Ikota	Masami	SuperSight	Perroots	Len
REC Silicon	Jap	Ren Heul	*SMS*	*Poduje*	*Noel*
Meiji University	Kawai	Naoyuki	Self	Sinha	Jaydeep
Sonoscan	Martell	Steve	I&I Consulting	Starikov	Alex
Tokyo Electron	Mashiro	Supika	*Self*	*Yoshise*	*Masanori*
JEOL	McIlwraith	Kevin			

Italic indicates remote participant

Table 2 Leadership Changes

WG/TF/SC/TC Name	*Previous Leader*	*New Leader*
Int'l AWG Task Force	Jaydeep Sinha is retired	

Table 3 Ballot Results

Document #	*Document Title*	*Committee Action*
5915	Line Item Revision to SEMI M1-1016: Specification For Polished Single Crystal Silicon Wafers (To add Illustration of Flatness Metrics for Silicon Wafers)	
	Line Item 1 - To add figures to newly provided Related Information 4 of M1 to illustrate the flatness metrics for silicon wafers and to add Table A1-1 to Appendix 1 with references for the figures added.	Passed with technical changes. Ratification Ballot will be issued in cycle 6-17.
6019A	Line Item Revision of SEMI M1-1016, Specification for Polished Single Crystal Silicon Wafers	

Table 3 Ballot Results

Document #	*Document Title*	*Committee Action*
	Line Item 1 - Change ¶R3-4.4 as follows to point out that minority carrier lifetime measurements in electronic silicon manufacture must be controlled by recombination at impurities	Passed as balloted
6041	Line Item Revision of M21-1110 Guide For Assigning Addresses To Rectangular Elements In A Cartesian Array	
	Line Item 1 - Changes to various related sections shown	Passed with editorial changes
6042A	Line Item Revision to SEMI MF1763-0706 (Reapproved 1111)Test Methods for Measuring Contrast of a Linear Polarizer (Title correction for conformance)	
	Line Item 1 - Correct title and concomitant text.	Passed as balloted
6096	Line Item Revision to SEMI M53-0216 Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodispere Reference Spheres on Unpatterned Semiconductor Wafer Surfaces	
	Line Item 1 - Addition of Related Information 2	Failed and will be reballoted
6169	Line Item Revision to MF1390-1014: Test Method For Measuring Bow And Warp On Silicon Wafer By Automated Noncontact Scanning	
	Line Item 1 - Delete Note 3 in section 2.5 and MF657 in section 4.1	Passed as balloted
	Line Item 2 - Deletion of Note 2 and modification of other sections as shown.	Passed as balloted

#1 **Passed** ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.

#2 **Failed** ballots and line items were returned to the originating task forces for re-work and re-balloting or abandoning.

Table 4 Activities Approved by the GCS between meetings of the TC Chapter

#	*Type*	*SC/TF/WG*	*Details*
None			

Table 5 Authorized Activities

#	*Type*	*SC/TF/WG*	*Details*
6205	SNARF	Int'l AWG TF	Line Item Revision to SEMI M43, Guide for Reporting Wafer Nanotopgraphy
6206	SNARF	Int'l AWG TF	Line Item Revision to SEMI M78, Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing
6207	SNARF	Int'l AWG TF	Line Items Revision to SEMI M1-1016, Add Shape metrics of Bow 3p in appendix 2 which was mistakenly removed at previous ballot, and add Illustrations of Shape Metrics for Silicon Wafers in Appendix 2.
tbd	SNARF	Int'l Polished Wafer TF	Reapproval of SEMI M8-0312, Specification for Polished Monocrystalline Silicon Test Wafers
tbd	SNARF	Int'l Polished Wafer TF	Reapproval of SEMI M38-0312, Specification for Polished Reclaimed Silicon Wafers
tbd	SNARF	Int'l Test Methods TF	Reapproval of • SEMI MF84-0312 - Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe

#	Type	SC/TF/WG	Details
			• SEMI MF95-1107 (Reapproved 1012) Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer • SEMI MF950-1107 (Reapproved 0912) Test Method for Measuring the Depth of Crystal Damage of a Mechanically Worked Silicon Wafer Surface by Angle Polished and Defect Etching • SEMI MF110-1107 (Reapproved 0912) Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique • SEMI MF1188-1107 (Reapproved 0912) Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption With Short Baseline • SEMI MF1388-0707 (Reapproved 0412) Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors • SEMI MF1392-0307 (Reapproved 0512) Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe • SEMI MF1527-0412 Guide for Application of Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon • SEMI MF1569-0307 (Reapproved 0512) Guide for Generation of Consensus Reference Materials for Semiconductor Technology • SEMI MF1617-0304 (Reapproved 0710) Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectrometry • SEMI MF1619-1107 (Reapproved 0912) Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle • SEMI MF1630-1107 (Reapproved 0912) Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities • SEMI MF2074-0912 Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers • SEMI MF374-0312 Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure • SEMI MF397-0812 Test Method for Resistivity of Silicon Bars Using a Two-Point Probe • SEMI MF523-1107 (Reapproved 1012) Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces • SEMI MF525-0312 Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe • SEMI MF576-0812 Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry • SEMI MF657-0707E Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning • SEMI MF671-0312 Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

#	Type	SC/TF/WG	Details
			• SEMI MF674-0705 (Reapproved 0611) Practices for Preparing Silicon for Spreading Resistance Measurements • SEMI M56-0307 (Reapproved 0512) Practice for Determining Cost Components for Metrology Equipment Due to Measurement Variability and Bias

NOTE 1: SNARFs and TFOFs are available for review on the SEMI Web site at: http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 6 Authorized Ballots

#	When	SC/TF/WG	Details
6205	Cycle 6-17	Int'l AWG TF	Line Item Revision to SEMI M43, Guide for Reporting Wafer Nanotopgraphy
6206	Cycle 6-17	Int'l AWG TF	Line Item Revision to SEMI M78, Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing
6096A	Cycle 6-17	Int'l AWG TF	Line Items Revision to SEMI M1-1016, Add Shape metrics of Bow 3p in appendix 2 which was mistakenly removed at previous ballot, and add Illustrations of Shape Metrics for Silicon Wafers in Appendix 2.
tbd	Cycle 7-17	Int'l Polished Wafer TF	Reapproval of SEMI M8-0312, Specification for Polished Monocrystalline Silicon Test Wafers
tbd	Cycle 7-17	Int'l Polished Wafer TF	Reapproval of SEMI M38-0312, Specification for Polished Reclaimed Silicon Wafers
tbd	Cycle 7-17	Int'l Test Methods TF	Reapproval of • SEMI MF84-0312 - Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe • SEMI MF95-1107 (Reapproved 1012) Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer • SEMI MF950-1107 (Reapproved 0912) Test Method for Measuring the Depth of Crystal Damage of a Mechanically Worked Silicon Wafer Surface by Angle Polished and Defect Etching • SEMI MF110-1107 (Reapproved 0912) Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique • SEMI MF1188-1107 (Reapproved 0912) Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption With Short Baseline • SEMI MF1388-0707 (Reapproved 0412) Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors • SEMI MF1392-0307 (Reapproved 0512) Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe • SEMI MF1527-0412 Guide for Application of Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

			• SEMI MF1569-0307 (Reapproved 0512) Guide for Generation of Consensus Reference Materials for Semiconductor Technology • SEMI MF1617-0304 (Reapproved 0710) Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectrometry • SEMI MF1619-1107 (Reapproved 0912) Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle • SEMI MF1630-1107 (Reapproved 0912) Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities • SEMI MF2074-0912 Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers • SEMI MF374-0312 Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure • SEMI MF397-0812 Test Method for Resistivity of Silicon Bars Using a Two-Point Probe • SEMI MF523-1107 (Reapproved 1012) Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces • SEMI MF525-0312 Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe • SEMI MF576-0812 Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry • SEMI MF657-0707E Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning • SEMI MF671-0312 Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials • SEMI MF674-0705 (Reapproved 0611) Practices for Preparing Silicon for Spreading Resistance Measurements • SEMI M56-0307 (Reapproved 0512) Practice for Determining Cost Components for Metrology Equipment Due to Measurement Variability and Bias

Table 7 SNARF(s) Granted a One-Year Extension

#	*TF*	*Title*	*Expiration Date*
None			

Table 8 SNARF(s) Abolished

#	*TF*	*Title*
None		

Table 9 Standard(s) to receive Inactive Status

Standard Designation	*Title*
SEMI M18-0912	Guide for Developing Specification Forms for Order Entry of Silicon Wafers
SEMI M32-0307 - (Reapproved 0512)	Guide to Statistical Specifications

Table 10 New Action Items

Item #	*Assigned to*	*Details*
July112017-#1	Kevin Nguyen and Tetsuya Nakai	To prepare Ratification ballot R5915, Line Item Revision to SEMI M1-1016: Specification For Polished Single Crystal Silicon Wafers (To add Illustration of Flatness Metrics for Silicon Wafers)
July112017-#2	Masanori Yoshise and Murray Bullis	To collaborate on M1 changes on shape decision tree including Bow 3p definition and Illustration.
July112017-#3	Dinesh Gupta	To email Junko Collins, copy Rich Allen, and Steve Martell on 5 year review for SEMI M71-0912 Specification for Silicon on Insulator Wafers for CMOS LSI for possible interest from Japan 3D committee
July112017-#4	Dinesh Gupta	To inform Murray Bullis on the GCS's decision to let SEMI M59 inactive

Table 11 Previous Meeting Action Items

Item #	*Assigned to*	*Details*	*Status*
April042017-#1	James Amano (SEMI Staff)	James Amano to ask TEM group to present to Silicon Wafer Committee at SEMICON West.	Completed
April042017-#2	Kurt Haller	Kurt Haller to contact Dieter Mueller regarding alternative reference for wafer flatness activity.	Completed
April042017-#3	Jaydeep Sinha	Jaydeep Sinha to send staff information on Future Fab article regarding wafer flatness.	Completed
April042017-#4	Kevin Nguyen (SEMI Staff)	Kevin Nguyen to send request for copyright release for wafer flatness article to Joanne Qiu/Intel	Completed

1 Welcome, Reminders, and Introductions

Dinesh Gupta called the meeting to order at 1:00 PM. The meeting reminders on antitrust issues, intellectual property issues and holding meetings with international attendance were reviewed. Attendees introduced themselves.

2 Review of Previous Meeting Minutes

The TC Chapter reviewed the minutes of the previous meeting.

Motion: Accept the minutes as written
By / 2nd: Fritz Passek/Kurt Haller
Discussion: None
Vote: 14-0

3 Liaison Reports

3.1 *Europe TC Chapter*

3.1.1 Fritz Passek reported for the Europe TC Chapter. Of note:

- Last meeting
  - Oct 26, 2016
  - SEMICON Europa
  - Grenoble, France
- Next meeting
  - Nov 2017
  - SEMICON Europa
  - Munich, Germany
  - Check www.semi.org/standards for latest update
- Task Forces with European Participation
  - Int'l Advanced Wafer Geometry (AWG) TF
  - Int'l Advanced Surface Inspection (ASI) TF
  - Int'l Terminology TF
  - Int'l Test Methods TF
  - Int'l Polished Wafer TF

Attachment: **01, Europe Si Wafer Liaison Report March 2017 v2**

3.2 *Japan TC Chapter*

3.2.1 Kevin Nguyen reported for the Japan TC Chapter. Of note:

- Last Meeting
  - June 16, Friday, 2017
  - SEMI Japan Office
- Next Meeting
  - 14:00-17:00, September 21, 2017
  - SEMI Japan Office
- JSNM/M4S
  - Japan Society of Newer Metals (JSNM), Material Standards Study Group for Semiconductor Supply-Chain(M4S)
  - Current Activities
    - Test method of low carbon concentration up to 5E14 atoms/cm3 in silicon by FT-IR
      - Round robin test is on going.

        - Test method of low carbon concentration up to 1E13 atoms/cm3 in silicon by PL
            - Test sample preparation is considering.
        - Test method of resistivity measurement of Si epitaxial layer with 1% accuracy
            - The activity above is just planned and not yet started

Attachment: 02, JA Si Liaison Report 2017 07 12 R0.2

3.3 *GCS*

3.3.1 Dinesh Gupta reported. Of note:

- SEMI M59 will go inactive when due for 5 year review
- Divide responsibility of reviewing SEMI Silicon Wafer standards. The concept is in agreement, details will need to be ironed out.

Attachment: 03, Silicon Wafer GCS Meeting, San Francisco 2017

3.4 *SEMI Staff Report*

3.4.1 Kevin Nguyen (SEMI) gave the SEMI Staff Report. Of note:

- Next meetings
    - November 6-9, 2017
        - SEMI HQ in Milpitas, California
- 2017 Critical Dates for SEMI Standards Ballots
    - Cycle 6, 2017
        - Ballot Submission Date: July 21
        - Voting Period Starts: August 1
        - Voting Period Ends: August 31
    - Cycle 7, 2017
        - Ballot Submission Date: August 18
        - Voting Period Starts: September 1
        - Voting Period Ends: October 2
- SEMI Standards Publications
    - Total SEMI Standards in portfolio: 974
        - Includes 191 Inactive Standards
        - Discussion: Dinesh feels the word inactive has a bad connotation toward the meaning of inactive standards even though they are still technically relevant. Kevin suggested Dinesh to provide suggestions to the Regs Subcommittee for consideration.

Attachment: 04, Staff Report July 2017_LN_SA v3

4 Regulations Change Report (if applicable)

4.1 There is no Regulations change.

5 Ballot Review

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.

Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

NOTE 2: TC Chapter adjudication on ballots reviewed is detailed in the Audits & Review (A&R) Subcommittee Forms for procedural review. The A&R forms are available as attachments to these minutes. The attachment number for each balloted document is provided under each ballot review section below.

5.1 Doc. 5915, Line Item Revision to SEMI M1-1016: Specification For Polished Single Crystal Silicon Wafers (To add Illustration of Flatness Metrics for Silicon Wafers)

5.1.1 Document passed with technical changes. Ratification ballot will be issued in cycle 6-17. See attachment below for details.

Attachment: 05, 5915 Procedural Review

5.2 Doc. 6019A, Line Item Revision of SEMI M1-1016, Specification for Polished Single Crystal Silicon Wafers

5.2.1 Document passed. See attachment below for details.

Attachment: 06, 6019A Procedural Review

5.3 Doc. 6041, Line Item Revision of M21-1110 Guide For Assigning Addresses To Rectangular Elements In A Cartesian Array

5.3.1 Document passed.

Attachment: 07, 6041 Procedural Review

5.4 Doc. 6042A, Line Item Revision to SEMI MF1763-0706 (Reapproved 1111)Test Methods for Measuring Contrast of a Linear Polarizer (Title correction for conformance)

5.4.1 Document passed.

Attachment: 08, 6042A Procedural Review

5.5 Doc. 6096, Line Item Revision to SEMI M53-0216 Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodispere Reference Spheres on Unpatterned Semiconductor Wafer Surfaces (Addition of a related information 2)

5.5.1 Document failed technical review.

Attachment: 09, 6096 Procedural Review (Failed Ballot)

5.6 Doc. 6169, Line Item Revision to MF1390-1014: Test Method For Measuring Bow And Warp On Silicon Wafer By Automated Noncontact Scanning

5.6.1 Document passed.

Attachment: 10, 6169 Procedural Review

6 Task Force Reports

6.1 Int'l Advanced Wafer Geometry Task Force /Noel Poduje (SMS), Jaydeep Sinha

6.1.1 Jaydeep reported two presentations took place

- Geometry Metrology Development Focus from Joann Qiu at Intel and
- Process Issues near notch on 300 mm wafers: G.Pfeiffer from Global Foundries

6.1.2 Ballot review

- 5915 - Line Item Revision to SEMI M1-1016. Ballot passed with technical change. Ratification ballot will be issued. Nakai and Kevin will coordinate to get the ballot out for next cycle.
- 6169 - Line Item Revision to MF1390-1014. Negative was found not persuasive. Ballot passed.

6.1.3 Ballot development

- SNARF for Line Item Revision to M49-1014, GUIDE FOR SPECIFYING GEOMETRY MEASUREMENT SYSTEMS FOR SILICON WAFERS FOR THE 130 nm TO 16 nm TECHNOLOGY GENERATIONS, Revise for 200mm metrology
- Development for M1 for adding illustrations of Shape metrics. Yoshise will propose changes on shape decision tree including Bow 3p definition and Illustration. SNARF was presented.

Motion: To approve M1 line item SNARF
By / 2nd: Kurt Haller/Len Perroots
Discussion: There was confusion on proposed changes for M1. Yoshise and Murray will hash it out.
Vote: 9-0. Motion passed.

- SNARF for Line item revision of M43/M78

Kurt Haller presented new source of reference in M43 and M78 for KV Ravi's document that need to be updated. The new reference was presented via a line-item change ballot.

Motion: To approve M43/M78 SNARFs
By / 2nd: Kurt Haller/Tetsuya Nakai
Discussion: None
Vote: 10-0. Motion passed.

Motion: To authorize line-item ballots for M43 and M78 for cycle 6-17 for review at SEMICON Europa
By / 2nd: Kurt Haller/Tetsuya Nakai
Discussion: None
Vote: 10-0. Motion passed.

6.1.4 Jaydeep Sinha reported that he is stepping down from being the TF leader. On behalf of the Silicon wafer committee, Noel Poduje sincerely expressed appreciation for Jaydeep's dedication and outstanding leadership.

Attachment: 11, AWG West 2017

6.2 Int'l Automated Advanced Surface Inspection Task Force/ Kurt Haller (KLA-Tencor)

6.2.1 Kurt reported ballot 6096, M53 Related Information 2 addition was found technically persuasive.

Motion: To authorize doc. 6096A cycle 6-17 for review at SEMICON Europa
By / 2nd: Kurt Haller/Len Perroots
Discussion: None
Vote: 9-0. Motion passed.

6.2.2 The TF also welcomed new participation from FemtoMetrix and Exnodes on inspection metrology topics. See attachments for details of presentations.

Attachment: 12, IAASIMinutes_10Jul2017 rev1

6.3 Int'l SOI Wafers TF/Gerd Pfeiffer (GlobalFoundries)

6.3.1 Dinesh Gupta reported two presentations were made at the meeting on

- Presentation on SOI Substrate Engineering for FDSOI Devices by C. Maleville
- Presentation on Materials and Characterization Issues in High Resistivity SOI for RF Applications by B. Standley

6.3.2 5 Year Review of SEMI M71-0912/ Specification for Silicon on Insulator Wafers for CMOS LSI

6.3.2.1 No activity for M71, however, Dinesh mentioned Japan may be still active. Rich Allen confirmed MEMS committee is not interested in SOI. However, Steve Martell mentioned there is potential interest in 3D Packaging and Integration committee in Japan. Dinesh will email Junko Collins and copy Steve and Rich.

Attachment: 13, SOI West 2017

6.4 Int'l Test Methods TF/Dinesh Gupta (STA)

6.4.1 Dinesh reported the following list of MF standards are due for 5 year review.

- SEMI MF84-0312 Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe
- SEMI MF95-1107 (Reapproved 1012) Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer
- SEMI MF950-1107 (Reapproved 0912) Test Method for Measuring the Depth of Crystal Damage of a Mechanically Worked Silicon Wafer Surface by Angle Polished and Defect Etching
- SEMI MF110-1107 (Reapproved 0912) Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique
- SEMI MF1188-1107 (Reapproved 0912) Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption With Short Baseline
- SEMI MF1388-0707 (Reapproved 0412) Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors
- SEMI MF1392-0307 (Reapproved 0512) Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe
- SEMI MF1527-0412 Guide for Application of Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon
- SEMI MF1569-0307 (Reapproved 0512) Guide for Generation of Consensus Reference Materials for Semiconductor Technology
- SEMI MF1617-0304 (Reapproved 0710) Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectrometry
- SEMI MF1619-1107 (Reapproved 0912) Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle
- SEMI MF1630-1107 (Reapproved 0912) Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities
- SEMI MF2074-0912 Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers
- SEMI MF374-0312 Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure
- SEMI MF397-0812 Test Method for Resistivity of Silicon Bars Using a Two-Point Probe
- SEMI MF523-1107 (Reapproved 1012) Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces
- SEMI MF525-0312 Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

- SEMI MF576-0812 Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry
- SEMI MF657-0707E Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning
- SEMI MF671-0312 Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials
- SEMI MF674-0705 (Reapproved 0611) Practices for Preparing Silicon for Spreading Resistance Measurements
- SEMI M56-0307 (Reapproved 0512) Practice for Determining Cost Components for Metrology Equipment Due to Measurement Variability and Bias

Motion: To issue reapproval ballots for the standards listed above for review at SEMICON Japan

By / 2nd: Dinesh Gupta/Tetsuya Nakai

Discussion: MF674 will be issued via title change to title conformance

Vote: 10-0. Motion passed.

6.4.2 Dinesh reported M18 and M32 are matured; further revisions are not needed, so these standards can go inactive.

Motion: To let M18 and M32 go inactive
SEMI M18-0912 - Guide for Developing Specification Forms for Order Entry of Silicon Wafers
SEMI M32-0307 - (Reapproved 0512) - Guide to Statistical Specifications

By / 2nd: Dinesh Gupta/Fritz Passek

Discussion: None

Vote: 9-0. Motion passed.

Attachment: 14, Min Test Methods TF Mtg 0717

6.5 Int'l Polished Wafers (Substrates) TF/John Valley

6.5.1 M8 and M38 are due for 5 year review, these standards should go out for reapproval ballot

Motion: To issue M8 and M38 for reapproval ballot for review at SEMICON Japan
SEMI M8-0312 - Specification for Polished Monocrystalline Silicon Test Wafers
SEMI M38-0312 - Specification for Polished Reclaimed Silicon Wafers

By / 2nd: Dinesh Gupta/Fritz Passek

Discussion: None

Vote: 9-0. Motion passed.

Attachment: 15, Min PW TF Mtg 0717

6.6 Int'l Terminology TF/TBD

6.6.1 No meeting. M59 will let go inactive. However, Murray has not been informed by the GCS decision. Dinesh will take the action item to communicate with Murray.

7 Old Business

None

8 New Business

8.1 Troy Morrison (Thermo Fisher Scientific) presented.

- Rationale for Transmission Electron Microscopy (TEM) Grids Standardization
    - TEM demand explodes to meet 3D transistor and multiple challenges

- Faster TEM data transition from lab to fab
- Lamella preparation and extraction from full wafers is automated
- Data acquisition (TEM imaging) and TEM metrology is automated
- But TEM grid transport between tools is manual, using tweezers
  - Requires operator interventions, and has a non-zero failure rate…
  - Is slow and not really compatible with FAB operation…
- Why standards?
  - Today the industry uses "3 mm grids" that have different form factors and do not respect a 'standard' for critical dimensions.
  - There are several TEM grid suppliers (Ted Pella,Omniprobe, Agar,…)
  - There are several TEM microscope suppliers (JEOL, Hitachi, FEI,..)
  - Our customers need to be able to buy FIB/SEM and TEM systems from different suppliers (mix and match, best-in-class)
    - compatibility between tools needs to be guaranteed
    - a TEM grid should be compatible with all FIB/SEM/TEM systems

- Scope of TEM-grid Standardization Survey
  - The questionnaire was sent to various stakeholders:
  - IC manufacturers
  - SEMI Standard Technical Members
    - PIC
    - Silicon Wafer
    - 3DS-IC)
- Results of TEM-grid Standardization Survey
  - A good response was obtained with all major IC manufacturers responding to the survey (n = 64)
  - 90% of current TEM sample handling is done manually and 75% of respondents would like to have it automated.
  - > 80% of respondents are in favor of having standard grids for:
    - Further automation (80%), TEM workflow efficiency (75%)
    - Compatibility between tools used in workflow (70%)
  - < 20% of respondents see drawbacks related to costs/compatibility
  - **> 80% of respondents are in favor of a SEMI standardization effort and 60% of respondents are willing to actively contribute to this effort**
- Discussion:
  - In term of time saving, how long is the entire process typically takes? [Len Perroots]
    - 30 min to 1 hr - for tool preparation
    - 1 hr – data extraction
    - 10 minutes – TEM data

  - The goal is not only it will save time, but to introduce automation in the process, which potentially eliminates human error. [Troy Morrison]
- Grid vendors are involved with the survey ? [Masami Ikota]
  - Yes. 5 grid vendors, 3 TEM vendors participated in the survey. [Troy Morrison]
- What is the ultimate goal? [Kurt Haller]
  - Elimination of human operator, introduction of automation, efficiency. Having the process automated, in case something goes wrong, root cause analysis can be identified. [Troy Morrison]
- Concern on patent, will there be any patent associated with the standard ? [Kevin McIlwraith]
  - There will be no commercial advantage; the goal is not to get in the grid business, but to create a TEM grid standard where it can be universally used.

Attachment: 16, TEM grid standardization

9 Next Meeting and Adjournment

9.1 The next meeting is scheduled for Tuesday, April 10, 2018 at SEMI HQ in Milpitas, CA. See http://www.semi.org/en/events for the current list of meeting schedules. Draft schedule for the next meeting is attached.

Attachment: 17, Sch SiWfr 0418 Tentative

Having no further business, a motion was made to adjourn. Adjournment was at 5:00 PM.

Respectfully submitted by:

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Minutes approved by:

Dinesh Gupta (STA)	<Date approved>
Noel Poduje (SMS)	<Date approved>

Table 12 Index of Available Attachments[#1]

Title	*Title*
Europe Si Wafer Liaison Report March 2017 v2	6169 Procedural Review
JA Si Liaison Report 2017 07 12 R0.2	AWG West 2017
Silicon Wafer GCS Meeting, San Francisco 2017	IAASIMinutes_10Jul2017 rev1
Staff Report July 2017_LN_SA v3	SOI West 2017
5915 Procedural Review	Min Test Methods TF Mtg 0717
6019A Procedural Review	Min PW TF Mtg 0717
6041 Procedural Review	TEM grid standardization
6042A Procedural Review	Sch SiWfr 0418 Tentative
6096 Procedural Review (Failed Ballot)	

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact [SEMI Staff Name] at the contact information above.