



Liaison Report for Japan TC Chapter of 3DS-IC Global Technical Committee

April 21, 2016 v0.1

To: Taiwan TC Chapter of 3DS-IC Global Technical Committee

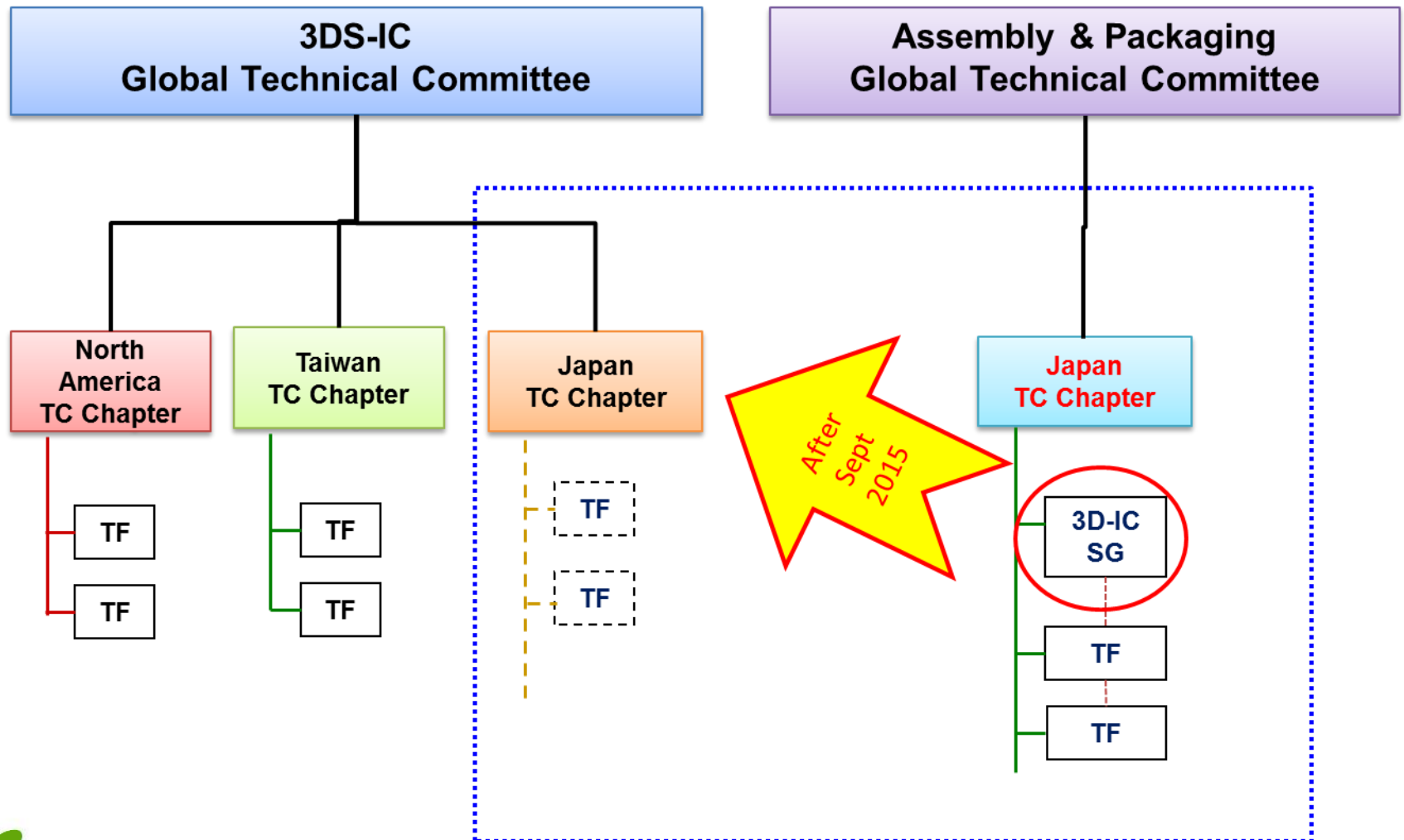
Outline

- Purpose of Formation of Japan TC Chapter of 3DS-IC Global Technical Committee
- Activities regarding 3DS-IC Issues in Japan Region
- Approval of Formation of 3DS-IC Japan TC Chapter and Leadership
- Current Organization Chart of 3DS-IC Japan TC Chapter
- Meeting Information
- TF / SG Updates
- Workshop for 3DS-IC Standardization
- Other 3DS-IC related activities in Japan

Purpose of Formation of Japan TC Chapter of 3DS-IC Global Technical Committee

- To enhance and reinforce the standard development activities as to solicit inputs from Japan members. ↓
- By soliciting proposals and inputs from Japanese members, to enhance and reinforce the 3DS-IC Standard Development Activities
- To interact with NA and Taiwan TC Chapters directly for further collaborations under the 3DS-IC Global Technical Committee.

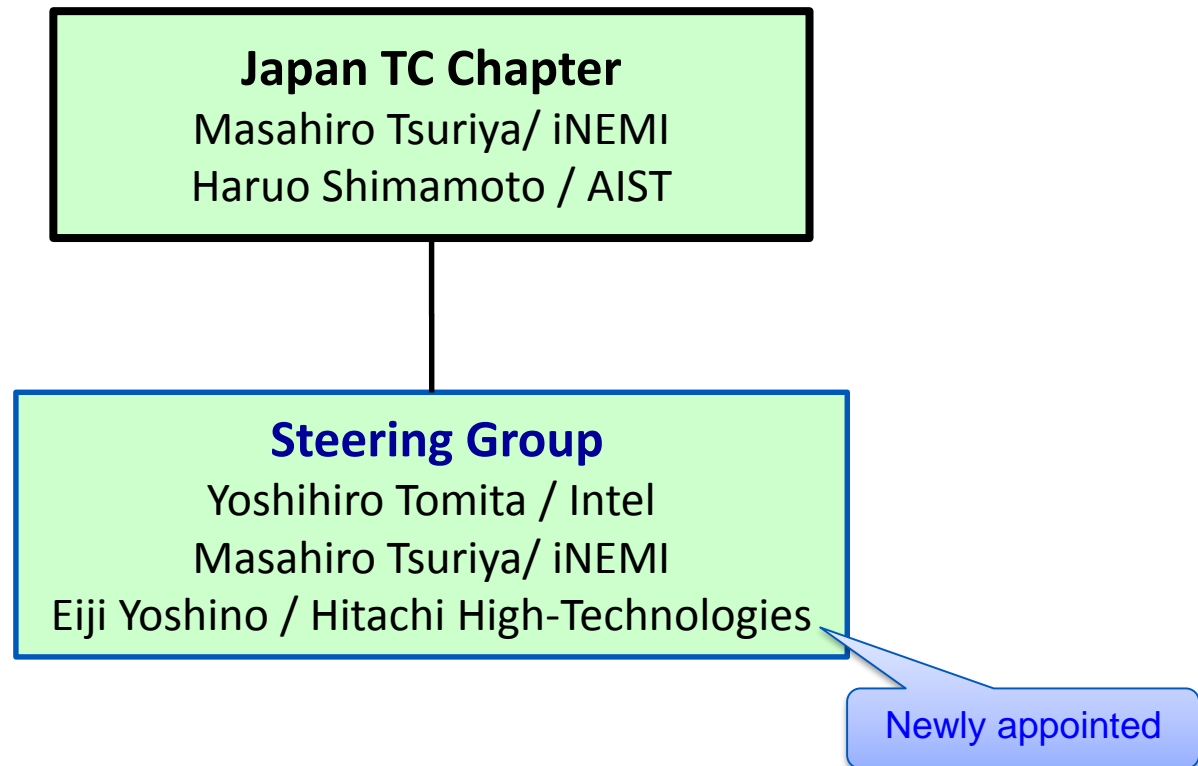
Activities regarding 3DS-IC Issues



Approval of Formation of 3DS-IC Japan TC Chapter and Leadership

- The formation of Japan TC Chapter of 3DS-IC Global Technical Committee was approved by JRSC at the meeting held on August 31, 2015.
 - The following leadership was also approved
 - Masahiro Tsuruya / iNEMI
 - Haruo Shimamoto / AIST

Current Organization Chart of Japan TC Chapter of 3DS-IC Global Technical Committee



Meeting Information

- Last Meeting – Japan Spring 2016 Meetings:
 - Friday, April 15, 2016
 - @ SEMI Japan office, Tokyo
- Next Meeting – Japan Fall 2016 Meetings:
 - Tuesday, September 6, 2016
 - @ SEMI Japan office, Tokyo

TF / SG Updates

- Steering Group
 - Approved at Kick-off meeting of 3DS-IC Japan TC Chapter held on Sept. 7, 2015
 - Leadership
 - Yoshihiro Tomita / Intel
 - Masahiro Tsuruya / iNEMI
 - Eiji Yoshino / Hitachi High-Technologies was newly appointed.
 - Charter
 - Define the work areas and review the global TC charter
 - Provide the following inputs and opportunities;
 - Plan technical workshop to promote the latest technologies and market trends on the 3DIC/SiP.
 - Brainstorm the areas of potential taskforce activities, and recommend the taskforce team formation to the Technical Committee
 - Handle any type of 3 dimensional IC package technologies including fan-out wafer level package or integrated SiP.
 - Provide the communication link from all layer of supply chain in Japan.
 - Interact with North America and Taiwan Technology Committee for the joint programs planning.

Workshops for 3DS-IC Standardization

- 1st Workshop
 - Held on Sept. 7, 2015 at SEMI Japan office
 - More than 60 attendees
 - Yole, ITRI, Tokyo Seimitsu and Toray Engineering made presentations
- 2nd Workshop
 - Held on January 12, 2016 at SEMI Japan office
 - More than 60 attendees
 - Yole, Otsuka Electronics and Hitachi Chemical made presentations
- 3rd Workshop
 - To be held on June 6, 2016 at SEMI Japan office
 - ITRI (tentative), Fujifilm and Toray Engineering to make presentations

Other 3DS-IC related activities in Japan

- Thin Chip Handling Task Force under Assembly & Packaging Japan TC Chapter
 - New Standard: SPECIFICATION FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
 - Doc. 5835 was published as SEMI G97-0116 in January 2016
 - SNARF for Line Item Revision to SEMI G97-0116 and the ballot submission to be proposed at the next Assembly & Packaging Japan TC Chapter on June 10, 2016
 - Doc. 5836: New Standard: TEST METHOD FOR ADHESIVE STRENGTH FOR ADHESIVE TRAY USED FOR THIN CHIP HANDLING
 - Ballot draft to be prepared

Thank you!

For more information about 3DS-IC Japan TC Chapter,
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