# North America Chapter
# 3DS-IC Global Technical Committee

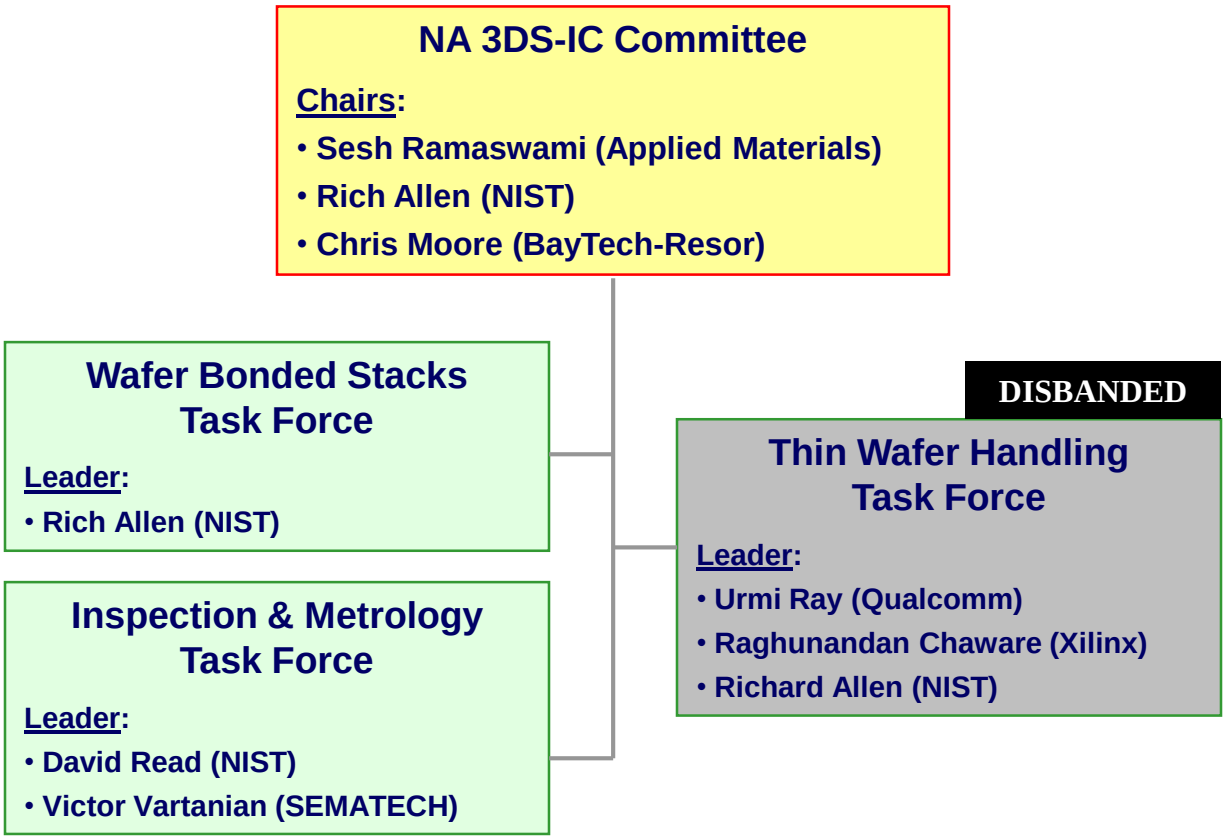
## Liaison Report

April 2016

# Leadership

- Committee Co-chairs
  - Rich Allen (NIST)
  - Chris Moore (BayTech-Resor)
  - Sesh Ramaswami (Applied Materials)

# Organization Chart



# Meeting Information

## NA 3DS-IC Committee

- Last meeting
  - April 5, 2016 at N.A. Standards Spring 2016 Meetings
    - SEMI Headquarters in San Jose, CA
- Next meeting
  - July 12, 2016 at SEMICON West 2016 Standards Meetings
    - San Francisco Marriot Marquis Hotel in San Francisco, CA

# Ballot Review Summary

## NA Spring 2016 Meetings

| *** Cycle 2, 2016 *** | | |
|---|---|---|
| Doc # | Description | TC Action |
| 5713 | New Standard: Specification For Glass Base Material For Semiconductor Packaging | **Failed** |

# Upcoming NA 3DS-IC Ballots

## To be reviewed at SEMICON West 2016 Meetings

| *** Voting Period – Cycle 4, 2016*** | | |
|---|---|---|
| Doc # | Document Title | Task Force |
| 5713A | New Standard: Specification for Glass Base Material for Semiconductor Packaging | Bonded Wafer Stacks TF |

# Task Force Updates [1/2]

- Bonded Wafer Stacks TF
  - Doc 5823A, Revision to SEMI 3D2-1113, *Specification for Glass Carrier Wafers for 3DS-IC Applications*
    - Published Feb 2016
  - Doc 5173, New Standard: *Guide for Describing Silicon Wafers for Use in a 300 mm 3DS-IC Wafer Stack*
    - Work ongoing – Granted one year extension at Spring Meetings
  - Doc 5713, New Standard: *Specification for Glass Base Material for Semiconductor Packaging*
    - Ballot Failed and returned to TF for re-work and will re-ballot in Cycle 4
  - Survey: Sealed MEMS Devices and Wafer Stacking
    - Survey has been distributed to MEMS/NEMS and 3DS-IC TC Members, and SEMI Global Update
    - Not many respondents; follow-up email to be sent out

# Task Force Updates [2/2]

- Inspection and Metrology TF
  - Doc 5822, New Standard: *Specification for Reference Material for Bonded Wafer Stack Void Metrology*
    - Work ongoing
  - SNARF for New Standard: *Terminology for 3DS-IC Technology*
    - GCS approval March 2016
    - Document #5976
    - Work ongoing

# Next NA 3DS-IC Meetings

[ Tentative ]

- SEMICON West 2016
- San Francisco Marriot Marquis Hotel in San Francisco, CA
  - Tuesday, July 12
    - Inspection & Metrology TF (9:00 AM to 10:30 AM)
    - Bonded Wafer Stacks TF (10:30 AM to 12:00 Noon)
    - NA 3DS-IC Committee (1:30 PM to 3:30 PM)

- Latest updates at:

  http://www.semi.org/en/standards-events

# Thank you!

- For more information, please visit the SEMI 3DS-IC Google Site:
  - https://sites.google.com/a/semi.org/3dsic/
- For more information or to participate in any NA 3DS-IC activities, please contact:
  - Laura Nguyen
    SEMI North America Standards
    lnguyen@semi.org

# Backup

# 3DS-IC Standards Committee

## Charter

- To explore, evaluate, discuss, and create consensus-based specifications, guidelines, and practices that, through voluntary compliance, will;
  - promote mutual understanding and improved communication between users and suppliers of 3DS-IC materials, carriers, automation systems and devices, and
  - enhance the manufacturing efficiency and capability and shorten time-to-market so as to reduce manufacturing cost in the 3DS-IC industry.

- Committee formed in Fall 2010
- Inaugural meeting held in January 12, 2011

# Participating Companies*

AGC Electronics

Altera

Applied Materials

Brewer Science

Corning

eda 2 asic

Elpida Memory

Entegris

Fujifilm Electronic

GLOBALFOUNDRIES

iNEMI

Intel

ITRI

Neocera

NIST

Novati

Qualcomm

Quartet Mechanics

ROHM Semiconductor

Rudolph Technologies

SEMATECH

Semilab

Shin-Etsu Polymer

Sonoscan

SUMCO

Suss MicroTec

Tezzaron

Toray Engineering

TSMC

Xilinx

* partial list

# Published Standards [1/13]

- SEMI 3D1-0912, *Terminology for Through Silicon via Geometrical Metrology*
  - Clear and commonly accepted definitions are needed for efficient communication and to prevent misunderstanding between buyers and vendors of metrology equipment and manufacturing services.
  - The purpose of this Document is to provide a consistent terminology for the understanding and discussion of metrology issues important to through silicon vias (TSV).

# Published Standards [2/13]

- SEMI 3D2-0216, *Specification for Glass Carrier Wafers for 3DS-IC Applications*
  - This Specification describes:
    - dimensional, thermal, and wafer preparation characteristics for glass starting material that will be used as carrier wafers in a temporary bonded state;
    - glass carrier wafers with nominal diameters of 200 and 300 mm, and a thickness of 700 um, although the wafer diameter and thickness required may vary due to process and functional variation. Such variations shall be clarified in the purchasing order or in the contract.
  - Methods of measurements suitable for determining the characteristics in the specifications are indicated.

# Published Standards [3/13]

- SEMI 3D3-0613, *Guide for Multi-Wafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames*
  - This Guide is intended to address the needs for choosing a method for shipping thin wafers on tape frames in such a way that they arrive undamaged at their final destination. It describes various methods of shipping thin wafers on tape frames.

# Published Standards [4/13]

- SEMI 3D4-0613, *Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks*
  - Control of parameters, such as bonded wafer stack (BWS) thickness, total thickness variation (TTV), bow, warp/sori, and flatness metrology, is essential to successful implementation of a wafer bonding process. These parameters provide meaningful information about the quality of the wafer thinning process (if used), the uniformity of the bonding process, and the amount of deformation induced to the wafer stack by the bonding process.
  - This Guide provides a description of tools that can be used to determine these key parameters before, during, and after the process steps involved in wafer bonding.

# Published Standards [5/13]

- SEMI 3D5-0314, *Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures*
  - This Guide aims to assist in the selection and use of tools for performing measurements of geometrical parameters of an individual TSV (through-silicon via), or of an array of TSVs.

# Published Standards [6/13]

- SEMI 3D6-0913, *New Standard: Guide for CMP and Micro-bump Processes for Frontside Through Silicon Via (TSV) Integration*
  - This Guide provides:
    - A generic middle-end process flow to define acceptable TSV and CMP quality criteria as well as to develop methodology and measuring procedures for micro-bump.
    - A criteria and common baselines of the middle-end process for related upstream and downstream manufacturers in fabricating 3DS-IC products.

Originated by Taiwan 3DS-IC

# Published Standards [7/13]

- SEMI 3D7-0913, *New Standard: Guide for Alignment Mark for 3DS-IC Process*
  - Photo alignment mark configuration is the key to ensure consistent and precise alignment of layers, chips and wafers.
  - This Guide provides:
    - the alignment mark strategy for chip to chip, chip to wafer, and wafer to wafer stacking.
    - addresses the universal alignment mark where the outcome will be a feasible photo alignment standard.

Originated by Taiwan 3DS-IC

# Published Standards [8/13]

- SEMI 3D8-0514, *Guide for Describing Silicon Wafers for Use as 300 mm Carrier Wafers in a 3DS-IC Temporary Bond-Debond (TBDB) Process*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure virgin silicon carrier wafers to be used in a 3DS-IC process.
- SEMI 3D9-0914, *Guide for Describing Materials Properties for a 300 mm 3DS-IC Wafer Stacks*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure wafer stacks to be used in a 3DS-IC process.

# Published Standards [9/13]

- SEMI 3D10-0814, *Guide to Describing Materials Properties for Intermediate Wafers for Use in a 300 mm 3DS-IC Wafer Stack*
  - This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure processed wafers to be used in a 3DS-IC process.

# Published Standards [10/13]

- SEMI 3D11-1214, *Terminology for Through Glass Via and Blind Via in Glass Geometrical Metrology*
  - This Document provides:
    - clear and commonly accepted definitions of through glass vias (TGV)
    - a consistent terminology for the understanding and discussion of metrology issues important them.
  - This Document focuses on geometry-related metrology and measurements important for definition and control of fabrication and inspection operations on structures that include openings for TGV.

# Published Standards [11/13]

- SEMI 3D12-0315, *Guide for Measuring Flatness and Shape of Low Stiffness Wafers*
  - This Guide provides:
    - Definitions for describing a more suitable measurement strategy for low stiffness wafers and geometries.
      - The more suitable measurement process consists of an alternative mounting for wafers with high aspect ratios and the use of high resolution measurements.
    - A measurement procedure for local bow, which denotes small areas of imperfection of the otherwise flat wafer or substrate.
      - This Guide's alternative measurement process is suitable for use in materials acceptance and process control, but may also be useful in other applications, such as wafer design and production.
    - This Document is a guide for a nondestructive procedure that uses a semi continuous flat mounting surface and high resolution measurement methods.

# Published Standards [12/13]

- SEMI 3D13-0715, *Measuring Voids in Bonded Wafer Stacks*
  - This Guide assists users in the selection and use of bond-void metrology equipment and a protocol for performing bond-void measurements based on their application.
    - New bonding processes and applications are sensitive to significantly smaller voids than bonding processes currently used for 3DS-IC package sealing.

# Published Standards [13/13]

- SEMI 3D14-0715, *Guide for Incoming/Outgoing Quality control and Testing Flow for 3DS-IC Products*
  - Background: To ensure consistent yield control of 3DS-IC products, common criteria for incoming quality control (IQC) and outgoing quality control (OQC) of outsourced subassembly and test (OSAT) are needed.
  - This Guide defines
    - the criteria for incoming quality control (IQC) and outgoing quality control (OQC) of OSATs, such as appearance, discoloration, missing ball or crack to clarify the manufacturer's responsibilities and to improve product yield.
    - the generic testing flows for different 3DS-IC products, such as chip on chip (CoC), chip on substrate (CoS), chip on wafer (CoW), stacked chip on substrate (SCoS), and wafer on wafer (WoW) to help accelerate the progress of 3DS-IC testing.
  - The generic testing flows for different 3DS-IC products also be defined in this Guide will expedite the progress of 3DS-IC testing.
- Also published:
  - SEMI AUX032-0715, *Round Robin Study of Method for Measurement of Voids in Bonded Pairs of Silicon Wafers*

# Published Standards [Packaging Volume]

- SEMI G96-1014, *Test Method for Measurement of Chip (Die) Strength by Mean of Cantilever Bending*
  - Defines a procedure for evaluation of die strength by mean of cantilever bending where 3 point bending is not easy to measure strength in case of wafer thickness less than 50 μm.
  - Applies only for cantilever bending method, and other methods will be defined by separate documents