North America 3DS-IC (Three-dimensional Stacked Integrated Circuits) Standards Committee Meeting Summary and Minutes

NA Standards Fall 2012 Meetings
30 October 2012, 15:00 – 17:00 Pacific Time
SEMI Headquarters in San Jose, California

Committee Announcements
Next Committee Meeting
NA Standards Spring 2013 Meetings
April 1-4, 2013
SEMI Headquarters in San Jose, California

Table 1 Meeting Attendees

Italics indicate virtual participants

Co-Chairs: Urmi Ray (Qualcomm), Sesh Ramaswami (Applied Materials), Chris Moore (Semilab), Richard Allen (SEMATECH)

SEMI Staff: Paul Trio

Company	*Last*	*First*	*Company*	*Last*	*First*
Applied Materials	Kumar	Niranjan	*SEMATECH*	*Vartanian*	*Victor*
BayTech Group	Baylies	Win	Semilab	Moore	Chris
BW & Associates	Wu	Bevan	Shin-Etsu Polymer	Kashimoto	Akira
Consultant	*Read*	*David*	Sonoscan	Martell	Steve
Corning	*Schmidt*	*Ilona*	TOK America	Rosenthal	Chris
Gran Systems	Ke	Kuang-Han	Xilinx	Chaware	Raghunandan
NIST	Cassard	Janet			
Pangrle Consulting	Pangrle	Suzette	SEMI	Trio	Paul
Quartet Mechanics	Jan	Feisa	SEMI Japan	Tejima	Naoko
SEMATECH	Allen	Richard			

Table 2 Leadership Changes

Group	*Previous Leader*	*New Leader*
Inspection & Metrology TF	Chris Moore (Semilab) stepped down as TF co-leader.	

Table 3 Ballot Results

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

Document #	*Document Title*	*Committee Action*
5173B	New Standard: Guide for Describing Materials Properties and Test Methods for a 300 mm 3DS-IC Wafer Stack	**Failed** and will be reballoted
5482	New Standard: Specification for Glass Carrier Wafers for 3DS-IC Applications	**Passed** as balloted. SUPERCLEAN

Table 4 Authorized Activities

#	*Type*	*SC/TF/WG*	*Details*
5506	SNARF	Inspection & Metrology TF	New Standard: Test Method for Measuring Warp, Bow and TTV on Silicon and Glass Wafers Mounted on Wire Grids by Automated Non-Contact Scanning using Laser Scanning Interferometry

Note: SNARFs and TFOFs are available for review on the SEMI Web site at:
http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 5 Authorized Ballots

#	When	SC/TF/WG	Details
5173C	Cycle 1, 2013	Bonded Wafer Stacks TF	New Standard: Guide for Describing Materials Properties for a 300 mm 3DS-IC Wafer Stack
5175	Cycle 1, 2013	Thin Wafer Handling TF	New Standard: Guide for Multi-Wafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames
5410	Cycle 1, 2013	Inspection & Metrology TF	New Standard: Guide for Metrology Techniques to be Used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures

Table 6 New Action Items

Item #	*Assigned to*	*Details*
None		

Table 7 Previous Meeting Actions Items

Item #	*Assigned to*	*Details*
None		

1 Welcome, Reminders, and Introductions

Chris Moore, committee co-chair, called the meeting to order at 3:07 PM. After welcoming all attendees, the SEMI meeting reminders on membership requirements, antitrust, patentable technology, and meeting guidelines were presented and explained. Finally, the agenda was reviewed.

Attachment: 01, SEMI Standards Required Meeting Elements

2 Review of Previous Meeting Minutes

The committee reviewed the minutes of the previous meeting held July 10 in conjunction with SEMICON West 2012.

Motion: Accept the minutes of the previous meeting as written.
By / 2nd: Steve Martell (Sonoscan) / Bevan Wu (BW & Associates)
Discussion: None

Vote: 10-0 in favor. Motion passed.

Attachment: 02, NA 3DS-IC SEMICON West 2012 meeting (July 10) minutes

3 SEMI Staff Report

Paul Trio (SEMI) gave the SEMI Staff Report. The key items were as follows:

- 2012 Global Calendar of Events
  - SEMICON Japan / PV Japan (December 5-7, Chiba)
- 2013 Global Calendar of Events (through July)
  - European 3D TSV Summit (January 22-23, Grenoble, France)
  - SEMICON/LED Korea (January 30 – February 1, Seoul)
  - ISS Europe 2013 [Industry Strategy Symposium] (February 24-26, Milan, Italy)
  - 7th PV Fab Manager Forum (March 10-12, Berlin, Germany)
  - SEMICON/FPD/SOLARCON China (March 19-21, Shanghai)
  - SEMICON Singapore (May 7-9, Marina Bay Sands)
  - SEMICON Russia (June 5-6, Moscow)
  - Intersolar Europe (June 19-21, Munich, Germany)
  - SEMICON West (July 9-11, San Francisco, California)
- NA Standards Fall 2012 Meetings
  - Committees meeting at SEMI Headquarters (San Jose)
    - 3DS-IC | EHS | Facilities & Gases | HB-LED | Information & Control | Liquid Chemicals | MEMS/NEMS | Metrics | PV/PV Materials | Traceability
  - SEMI thanks Intel (Santa Clara) for hosting the PIC and Silicon Wafer meetings
- NA Standard Spring 2013 Meetings
  - April 1-4 at SEMI Headquarters in San Jose, California
  - Inviting local companies willing and able to host some of the meetings to maintain one-week format
  - Final schedule to be announced by the end of December 2012
- Technical Ballot Critical Dates for NA Spring 2013 Meetings
  - Cycle 1: due January 3 / January 16 – February 15
  - Cycle 2: due February 4 / February 18 – March 20
- Upcoming NA Meetings
  - NA HB-LED Task Force Meetings @ Strategies in Light
    - February 12-14, 2013 in Santa Clara, California
  - NA Microlithography Committee Meeting @ SPIE Advanced Lithography
    - February 24-28, 2013 in San Jose, California
  - NA Standards Spring 2013 Meetings
    - April 1-4, 2013 in San Jose, California
- Standards Publications Report
  - July 2012 Cycle
    - New Standards – 6, Revised Standards – 6, Reapproved Standards – 4, Withdrawn Standards – 2
  - August 2012 Cycle
    - New Standards – 0, Revised Standards – 16, Reapproved Standards – 7, Withdrawn Standards – 0

  - September 2012 Cycle
    - New Standards – 10, Revised Standards – 18, Reapproved Standards – 7, Withdrawn Standards – 0, Total in portfolio – 860 (includes 92 Inactive Standards)
- New Ballot Formatting Templates
  - Updated 2010 versions to comply with Style Manual and Procedure Guide changes
  - Templates by Document subtypes are available on the SEMI Standards web site, includes the mandatory sections for each type
- Style Manual
  - Version 5 published in August 2011
  - Major changes: Required sections information moved to the Procedure Guide; Notices updated
  - The Style Manual contains terminology formatting information; the Procedure Guide contains information about writing/attributing definitions
- Compilation of Terms (COT)
  - Updated and published after each publication cycle is completed
  - Contains all Abbreviations, Acronyms, Definitions and Symbols listed in the terminology section of Standards and Safety Guidelines.
- Coming Soon: New Standards Ballot and Membership Systems. Key changes:
  - User interface
  - Log-in
    - One-time log-in per session to vote on ballots
    - Same log-in for SEMI Members
  - Functionality
    - Retrieve and edit submitted votes for current cycle
    - Text field and attachment option for each ballot or line item
  - Integration
    - Linked to new membership application / profile management
    - Access to other SEMI products & services

  Target deployment: Cycle 1, 2013

Attachment: 03, SEMI Standards Staff Report

4 Taiwan 3DS-IC Committee

Paul Trio (SEMI) gave the Taiwan 3DS-IC Report. The key items were as follows:

- Leadership
  - TK Ku (ITRI) | Wendy Chen (KYEC) | Yi-Shao Lai (ASE)
- Next meeting
  - November 26, 2012 in Hsinchu (ITRI)
- 3DS-IC Testing TF
  - Formed on October 26, 2011
  - Charter: The Testing Task Force will develop standards, guidelines, and/or specifications for electrical testing related activities used in 3DS-IC manufacturing for the ultimate goal of yield enhancement.
  - Scope: Activities related to electrical testing of prebond and bonded wafers/devices include (but not limited to):
    - Design for Test (DfT) such as test structures and placement;

  - Test methodologies such as contact method and test procedures;
  - Test fixtures such as probe card and probe interfaces, and
  - Data mining test results
- Middle-End Process TF
  - Formed on February 9, 2012
  - Charter: Develop the standards and define the specifications for middle-end process (MEOL) related manufacturing flow. Current Phase of Standard and Specification development focused on the middle-end process on wafers with or without TSVs, including post final metal temporary bonding, wafer thinning, TSV formation and reveal, micro-bumping, redistributed line (RDL) formation and carrier de-bond.
  - Scope:
    - Identify and suggest generic process flow for middle-end process.
    - Develop criteria for micro-bump dimensions, planarization and related. Dimensions can be determined into wafer-to-wafer level (WWL), die-to-wafer level (DWL), and die-to-die level (DDL).
    - Develop criteria for TSV CMP process and related. The via size, via surface roughness, post CMP Cu step height, and post CMP Cu bump planarization uniformity are a few of the related planarization criteria that will be critical to the micro bumping yield and inspection standard.
    - Develop standard for photo alignment mark and overlay mark. Alignment marks for patterning TSVs and stacking devices/wafers would be standardized for recognition.
    - Suggest wafer or die thickness variation and warpage before and after MEOL and identify thickness variation, void size, overall void percentage of temporary bonding glue layer, warpage control after temporary bonding and corresponding measure method.
    - Develop TSV quality criteria such as thickness uniformity, TSV depth variation, void, pattern density, TSV metal extrusion.
    - Research on in-process testing.
- New SNARF:
  - 5485 – New Standard: Guide for Incoming/Outgoing Quality Control and Testing Flow for 3DS-IC Products
    - Task Force: Testing TF
    - Rationale: To ensure consistent yield control of 3DS-IC products, common criteria for incoming quality control (IQC) and outgoing quality control (OQC) of OSATs (outsourced sub-assembly and test providers) are needed. The generic testing flows for different 3DS-IC products to also be defined in this document will expedite the progress of 3DS-IC testing.
    - Scope: This guide will define the criteria of incoming quality control (IQC) and outgoing quality control (OQC) of OSATs, such as appearance, TSV void percentage by X-ray inspection, etc., to clarify the manufacturer's responsibilities and to improve product yield.

      This guide will also define the generic testing flows for different 3DS-IC products, such as chip on chip (CoC), chip on substrate (CoS), stacked chip on substrate (CoS), wafer on wafer (WoW), etc., to help accelerate the progress of 3DS-IC testing.
- Existing SNARFs:
  - 5473 – New Standard: Guide for Alignment Mark for 3DS-IC Process
    - Task Force: Middle-End Process TF
    - Rationale: To ensure consistent precise alignment of layers, chips and wafers, the photo alignment mark configuration is the key and should be developed. Therefore, the guide will provide alignment mark strategy for die to die, die to wafer, and wafer to wafer

stacking. This guide will address the universal alignment mark where the outcome will be a feasible photo alignment standard.

    - Scope: Define and develop litho alignment strategy for die to die (DDL), die to wafer (DWL) and wafer to wafer (WWL) stacking. The alignment mark is preferred to be implemented at front side final metal and/or backside metal layer masking. This guide will address universal alignment mark, including shape, dimension, and location will be proposed. The outcome of a feasible photo alignment standard will be critical to the DDL, DWL and WWL stacking.
  - 5474 – New Standard: Guide for CMP and Micro-bump Processes for Frontside TSV Integration
    - Task Force: Middle-End Process TF
    - Rationale: To speed up the volume production of 3DS-IC products, a generic middle-end process flow is needed to communicate the frontend and backend processes. The quality criteria and metrology methodology of the key modules such as TSV, CMP and micro-bump are developed to ensure the high yield of the middle-end process. Therefore, this guide will suggest generic middle-end process flow to define acceptable TSV and CMP quality criteria, and develop methodology and measuring procedure for micro-bump. The guide will provide criteria and common baselines of the middle-end process for related upstream and downstream manufacturers in fabricating the 3DS-IC products.
    - Scope: Propose a frontside TSV integration scheme as one of the generic middle-end process flow. The flow includes steps such as TSV formation, RDL formation, CMP, temporary carrier bonding, wafer thinning, micro-bump formation, carrier debonding, etc.

      Define acceptable CMP criteria of TSV in terms of dishing, erosion, and voids. CMP criteria can be determined by metrology technology such as Alpha stepper, Ultrasonic, Coherence Interferometry, and etc. TSV formation and reveal are significantly dependent on the performance of CMP process. The outcome of the high CMP quality yields better TSV connectivity.

      Develop criteria for measurement methodology for micro-bump dimensions, including sampling rate, sampling sites and mapping, reference datum, and survey available metrology tools. The outcome will be an important bridge communication between IC design firms and associated foundry and packaging fabs. The assumption of DWL and DDL are that testing data is available for known good die status.

- SEMI Staff:
  - Catherine Chang | cchang@semi.org

Attachment: 04, Taiwan 3DS-IC Report

5 Japan 3D-IC Study Group

Naoko Tejima (SEMI Japan) gave the 3D-IC Study Group presentation. The key items were as follows:

- Formed under the Japan Packaging Committee
- Study Group leaders
  - Kazunori Kato (AiT) | Yutaka Koma (Koma Consulting) | Masahiro Tsuriya (iNEMI)
- The kick off meeting was held on October 5. All TFOF and SNARFs from NA and Taiwan were reviewed
- Next meeting: November 7. Agenda: Discuss plan for future activities in Japan
- Planning global meeting with NA and TW members at the next committee meeting on December 6, in conjunction with SEMICON Japan 2012
  - Purpose:
    - Establish networking with North America/Taiwan 3DS-IC committee to accelerate the development of standards for the needs for 3D-IC manufacturing materials and processes

    - Identify area for Japan taskforce team to work on for the creation of documents through the collaboration with North America / Taiwan committees
  - Meeting Agenda (draft):
    - Status of Japan industries on 3D-IC market and technology
    - Discussion about the potential area to be standardized on 3D-IC manufacturing materials and processes
    - Discussion about the drafted scope and work plan for Japan team
    - Understanding on the scope of North America and Taiwan committees
    - Open Discussion
- SEMI Staff:
  - Naoko Tejima | ntejima@semi.org

Attachment: 05, Japan 3D-IC Study Group Presentation

6 Ballot Review

Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

NOTE 1:Committee adjudication on Cycle 6 ballots are detailed in the Audits & Reviews (A&R) Subcommittee Forms for procedural review. These A&R forms are available as attachments to these minutes. The attachment number for each document is provided below the summary tables.

6.1 *Cycle 6 Ballots*

Document #	*Document Title*	*Committee Action*
5173B	New Standard: Guide for Describing Materials Properties and Test Methods for a 300 mm 3DS-IC Wafer Stack	**Failed** and will be reballoted
5482	New Standard: Specification for Glass Carrier Wafers for 3DS-IC Applications	**Passed** as balloted. SUPERCLEAN

Attachment: 06, Ballot Review for Doc. 5173B

07, Ballot Review for Doc. 5482

7 Task Force Reports

7.1 *Bonded Wafer Stacks Task Force*

Rich Allen (SEMATECH) reported that the task force will review feedback received on ballot 5173B.

7.2 *Inspection & Metrology Task Force*

Rich Allen reported that the task force reviewed Documents 5409 [*New Standard: Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks*] and 5410 [*New Standard: Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures*] with plans to ballot for the Cycle 1, 2013 voting period. The TF will also submit a new SNARF for committee approval (see section 9.1 of these minutes). Finally, Rich reported that the TF is still working on Documents 5270 (*New Standard: Guide for Measuring Voids in Bonded Wafer Stacks*) and 5447 (*Terminology for Measured Geometrical Parameters of Through-Glass Vias (TGVs) in 3DS-IC Structures*).

7.3 *Thin Wafer Handling Task Force*

Rich Allen reported that the TF plans to ballot Document 5175 (*New Standard: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers*) for the Cycle 1, 2013 voting period.

8 Old Business

8.1 Completed action Items from previous meeting:

Item #	*Assigned to*	*Action Item*	*Status*
None			

9 New Business

9.1 *New TFOFs & SNARFs*

Ilona Schmidt (Corning) presented a new SNARF from the Inspection & Metrology TF to the committee for approval:

New Standard: Test Method for Measuring Warp, Bow and TTV on Silicon and Glass Wafers Mounted on Wire Grids by Automated Non-Contact Scanning using Laser Scanning Interferometry

- Rationale:
    - The current metrology strategies have evolved from methods used to characterize smaller, lower aspect ratio geometries. Conventionally, three point mounts have been used to measure flatness/warp of wafer along with the gravity compensation.
    - For instance 3DS-IC applications use larger and thinner wafers than conventional applications. Large, thin wafers have inherently low stiffness, leading to large deflections, which make compensation more challenging. Ball mounts cause large deflections, 4-point and ring supports have redundant support and are sensitive to how parts are placed on the mount.
    - The industry therefore would benefit from identifying an alternate test method that better reflects the application usage of these wafers. One such approach used in the industry is a similar set up to Sori with a wire mount and a noncontact scanning method that allows depicting a complete picture of the wafer's shape and dimensional parameters.
    - This method will recommend the wafer to be characterized in a position that allows for a free state profile measurement on a flat surface.
- Scope:
    - Describe a test method that accurately and reliably depicts the dimensional shape of single silicon and glass wafers that are ≥ 300 mm in diameter and ≤ 775 µm in thickness and that uses a wire mount and Laser scanning interferometry.
    - The document will include applicable ranges for valid measurements where possible.

Motion: Approve SNARF: *New Standard: Test Method for Measuring Warp, Bow and TTV on Silicon and Glass Wafers Mounted on Wire Grids by Automated Non-Contact Scanning using Laser Scanning Interferometry*

By / 2nd: Richard Allen (SEMATECH) / Steve Martell (Sonoscan)

Discussion: Chris Rosenthal (TOK America) asked why this activity does not include stacked wafer. Chris Moore (Semilab) responded that the goal is to narrow the scope enough so that it would be easier to get it through the process. Furthermore, he pointed out that this activity would establish a baseline for other test methods in the future. Nevertheless, Chris Moore agreed that there should be a test method for stacked wafer.

Vote: 8-0 in favor. Motion passed.

9.2 *Upcoming Ballots*

#	*Type*	*SC/TF/WG*	*Details*
5173C	Cycle 1, 2013	Bonded Wafer Stacks TF	New Standard: Guide for Describing Materials Properties for a 300 mm 3DS-IC Wafer Stack
5175	Cycle 1, 2013	Thin Wafer Handling TF	New Standard: Guide for Multi-Wafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames
5410	Cycle 1, 2013	Inspection & Metrology TF	New Standard: Guide for Metrology Techniques to be Used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures

Motion: Approve letter ballot distribution of document 5173C for the Cycle 1, 2013 voting period.
By / 2nd: Richard Allen (SEMATECH) / Steve Martell (Sonoscan)
Discussion: None
Vote: 8-0 in favor. Motion passed.

Motion: Approve letter ballot distribution of document 5175 for the Cycle 1, 2013 voting period.
By / 2nd: Richard Allen (SEMATECH) / Steve Martell (Sonoscan)
Discussion: None
Vote: 8-0 in favor. Motion passed.

Motion: Approve letter ballot distribution of document 5410 for the Cycle 1, 2013 voting period.
By / 2nd: Richard Allen (SEMATECH) / Suzette Pangrle (Pangrle Consulting)
Discussion: None
Vote: 6-0 in favor. Motion passed.

Action Item Review

9.3 *Open Action Items*

Paul Trio (SEMI) reviewed the open action items. These can be found in the Open Action Items table at the beginning of these minutes.

9.4 *New Action Items*

Paul Trio (SEMI) reviewed the new action items. These can be found in the New Action Items table at the beginning of these minutes.

10 Next Meeting and Adjournment

The next meeting of the North America 3DS-IC committee is scheduled for Tuesday, April 2 in conjunction with the NA Standards Spring 2013 meetings. The tentative schedule is provided below:

North America Standards Spring 2013 Meetings
April 1-4, 2013
SEMI Headquarters
3081 Zanker Road
San Jose, CA 95134
U.S.A.

Tuesday, April 2

- Inspection & Metrology Task Force (8:00 AM to 10:00 AM)
- Wafer Bonded Stacks Task Force (10:00 AM to 12:00 Noon)
- Thin Wafer Handling Task Force (1:00 PM to 3:00 PM)
- NA 3DS-IC Committee (3:00 PM to 5:00 PM)

Having no further business, a motion was made to adjourn the NA 3DS-IC Committee meeting in conjunction with the NA Standards Fall 2012 meetings in San Jose, California. Adjournment was at 4:35 PM.

Respectfully submitted by:

Paul Trio
Senior Manager, Standards Operations
SEMI North America
Phone: +1.408.943.7041
Email: ptrio@semi.org

Minutes approved by:

Sesh Ramaswami (Applied Materials), Co-chair	Not present
Urmi Ray (Qualcomm), Co-chair	Not present
Richard Allen (SEMATECH), Co-chair	January 2, 2012
Chris Moore (Semilab), Co-chair	

Table 8 Index of Available Attachments [#1]

#	*Title*	*#*	*Title*
1	SEMI Standards Required Meeting Elements	5	Japan 3D-IC Study Group Presentation
2	NA 3DS-IC West 2012 Meeting (July 10) Minutes	6	Ballot Review for Doc. 5173B
3	SEMI Standards Staff Report	7	Ballot Review for Doc. 5482
4	Taiwan 3DS-IC Report		

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Paul Trio at the contact information above.