NA Silicon Wafer Committee Meeting Minutes

NA Spring Standards Meetings 2013
Tuesday, 2 April, 2013, 1:00 PM - 4:00 PM
Intel, Santa Clara, CA

Next Committee Meeting
July 9, 2013, San Francisco Marriott Marquis, CA in conjunction with SEMICON West Standards Meetings. Check www.semi.org/standards for the latest update.

Attendees:

SEMI Staff
Kevin Nguyen – SEMI NA

Co-chair – Dinesh Gupta (STA)

Table 1 – Meeting Attendees

Last Name	*First Name*	*Company*
Bullis	Murray	Materials & Metrology*
Goldstein	Mike	Intel
Kren	George	KLA-Tencor
Lee	KwangWook	G450C
Nakai	Tetsuya	SUMCO
Perroots	Len	SuperSight
Poduje	Noel	SMS*
Shimizu	Yasuhiro	Consultant*
Sinha	Jaydeep	KLA-Tencor
Sotirov	Zlatko	Genmark Automation
Swirhun	James	Sinton Instruments

*Attended via teleconference

Table 2 – Leadership Changes
None

Table 3 – Ballot Summary
Passed ballots and line items will be submitted to the ISC Audit & Review Subcommittee for procedural review.
Failed ballots and line items were returned to the originating task forces for re-work and re-balloting.

Document #	*Document Title*	*Committee Action*
5450A	Revision to SEMI M49-0912, Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 22 nm Technology Generations with Title Change to: Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations	Passed as balloted
5559	New Auxiliary Information: Interlaboratory Evaluation Of Nondestructive Method For Measuring The Edge Contour Of Silicon Wafers	Approved by the Committee
5430A	Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles	To be adjudicated at SEMICON West 2013

Table 4 – Authorized Ballots

#	*When*	*SC/TF/WG*	*Details*
5543	Cycle 4-2013	Int'l Polished Wafer TF	Line Items Revision to SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers
5541	Cycle 4-2013	Int'l SOI Wafer TF	Revision of SEMI M41-0707, Specification of Silicon-on-Insulator (SOI) for Power Device/Ics

Table 5 – Authorized Activities

#	*Type*	*SC/TF/WG*	*Details*
5543	SNARF	Int'l Polished Wafer TF	Line Items Revision to SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers (SNARF was revised to allow additional line item changes)
5583	SNARF	Int'l Annealed Wafer TF	Revision of SEMI M57-0413, Specifications for Silicon Annealed Wafers

Note: SNARFs and TFOFs are available for review on the SEMI Web site at: http://downloads.semi.org/web/wstdsbal.nsf/TFOFSNARF

Table 6 – Previous Meeting Actions Items

Item #	*Assigned to*	*Details*	*Status*
None			

Table 7 – New Actions Items

Item #	*Assigned to*	*Details*
0413-1	Kevin Nguyen (SEMI Staff)	To email George Kren regarding SEMI M35-1107 Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection, which is due for 5 year review
0413-2	Kevin Nguyen (SEMI Staff)	To send JEITA round robin samples to Japan SEMI Staff for transferring to AIST

1. Call to Order

Dinesh Gupta called the meeting to order and welcomed everyone who attended. A round of self introduction was made. All SEMI standards meetings are subjected to SEMI Anti-Trust Reminder and Guidelines concerning Patentable Technology. SEMI Regulations now require all attendees to be members of SEMI standards. Membership enrollment is at www.semi.org/standardsmembership. Agenda was reviewed and proceed as shown.

2. Review of Schedule for the Next Meeting (SEMICON West, July 8-9, 2013)

The next meeting will be in San Francisco, CA scheduled for July 8-9, 2013 in conjunction with SEMICON West Standards Meetings. Check www.semi.org/standards on the calendar of entry for the latest schedule and meeting location. Tentative schedule for the next meeting is as follows:

Monday, July 8, 2013

Time	Meeting Name
08:30-09:30	Int'l SOI (TF)
09:30-10:30	Int'l Annealed Wafer (TF) & Int'l Epi Wafer (TF)
10:30-11:00	Int'l Terminology (TF)
11:00-12:00	Int'l Advanced Surface Inspection (TF)
12:00-13:00	GCS (Invitation Only)
13:00-15:30	Int'l Advanced Wafer Geometry (TF)
15:30-17:30	Int'l Test Methods (TF)

Tuesday, July 9, 2013

Time	Meeting Name
08:30-10:00	Int'l Polished Wafer (TF)
10:00-12:00	Int'l 450 mm Wafer (TF)
13:00-17:00	Silicon Wafer (C)

3. Review and Approval of the Minutes from NA Fall meeting, October 30, 2012 in Santa Clara, CA

The meeting minutes reviewed. No change was made.

Motion: Accept the minutes of the previous meeting as submitted
By / 2nd: Jaydeep Sinha (KLA-Tencor)/Mike Goldstein (Intel)
Discussion: None
Vote: Unanimous. Motion passed

Attachment – 1, Minutes NA SiWfr 20121030

4. Liaison Reports

4.1. Europe Committee

Report was given by Kevin Nguyen. Highlights.

- Last Meeting
  - October 9-11, 2012 in conjunction with SEMICON Europa, Dresden, Germany
- Next Meeting
  - October, 2013 in conjunction with SEMICON Europa, Dresden, Germany
  - Check www.semi.org/standards calendar of event for latest update
- EU Silicon Wafer Committee
  - New Leader
    - Friedrich Passek (Siltronic)
- Int. Advanced Wafer Geometry TF
  - Meeting Berlin on March 13, 2013
  - Doc 5430A, Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles: passed ballot without negatives or comments
  - Revisions of SEMI M1 on-going
  - New auxiliary document illustrating flatness metrics under development
- Int. Polished Wafer TF
  - Meeting in Berlin, March 13, 2013
  - New draft document under development: Specification for Polished Single Crystal Silicon Wafers for GaN-on-Silicon Applications
- Int. Test Methods TF
  - No meeting in Europe for a while
  - Interaction with Japanese and NA TFs regarding
    - Doc 4846C, Revision to MF1982,Test method for Analyzing Organic Contaminants on Silicon Wafer Surface by Thermal Desorption Gas Chromatography, and
    - Doc 4844B, Guide for the measurement of trace metal contamination on silicon wafer surface by inductively coupled plasma mass spectrometry
    - Doc 5313C, Revision to MF1535, µPCD measurement

Attachment – 2, EU Si Wafer liaison report_March 2013

4.2. Japan Committee

Tetsuya Nakai (SUMCO) reported. Highlights.

- Last Meeting
  - March 8, 2013 at SEMI Japan, Tokyo
- Next Meeting
  - June 7, 2013 at SEMI Japan, Tokyo

- Ballots resulted from SEMICON Japan meeting

Document #	*Document Title*	*Committee Action*
5252A	Revision of SEMI M57-1011 with Title Change To: Specifications for Silicon Annealed Wafers	**Passed** with editorial changes
5442	Reapproval of SEMI M74-1108, Specification for 450 mm Diameter Mechanical Handling Polished Wafers	**Passed** as balloted (Super clean)
5441	Line Items Revision of SEMI M1-0812, Specifications for Polished Single Crystal Silicon Wafers	**Passed**.
5448	Revision of SEMI MF1528-0308, Test Method for Measuring Boron Contamination in Heavily Doped N-Type Silicon Substrates by Secondary Ion Mass Spectrometry	**Passed** as balloted (Super clean)
5449	Reapproval of SEMI MF1049-0308, Practice for Shallow Etch Pit Detection on Silicon Wafers	**Passed** as balloted (Super clean)
5451	Reapproval of SEMI MF1366-0308, Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry	**Passed** as balloted (Super clean)
5313B	Line Item Revisions of SEMI MF1535-0707, Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance	**Failed** and turned to the Task Force for rework.
5424A	Line Items Revision to SEMI M62-0912, Specifications for Silicon Epitaxial Wafers	See below.
Line Item 1	Revision of Tables R2-7 & R2-8 - Change ¶3-1.7	**Passed** as balloted (Super clean)
Line Item 2	Revision of Tables R2-7 & R2-8 - Change ¶3-2.7 and explanation #9	**Failed** and turned to the Task Force for rework.
5450	Revision to SEMI M49-0912, Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 22 nm Technology Generations with Title Change to: Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations	**Failed** and turned to the Task Force for rework.

- Japan Test Method Task Force
  - Drafting
    - Doc. 5389, Revision to SEMI MF1982, Test method for analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography
    - Doc. 4844B, New Standard: Guide for the Measurement of Trace Metal Contamination on Silicon Wafer Surface by Inductively Coupled Plasma Mass Spectrometry.
  - The TF plans for next work as revision of M60, Test Method for Time Dependent Dielectric Breakdown Characteristics of SiO2 Films for Si Wafer Evaluation.
- SEMI Standards Technical Education Program (STEP) on 450 mm Wafer at SEMICON Japan 2012
  - It drew more than 60 participants.
- Discontinuance of the JEITA Si Technology Committee and Transfer of JEITA Standards to SEMI
  - See details in attachment below
- Hirofumi Kanno, SEMI Japan (hkanno@semi.org)

Attachment: 3, JP_SiW_NA Spring_R0.1

5. Staff Report

Report was given by Kevin Nguyen. Highlights:

- 2013 Event

Event Name	*Event Details*
SEMICON West	July 9-11, 2013 San Francisco, California
SEMICON Taiwan	September 4-6, 2013 Taipei
SEMICON Europa	October 8-10, 2013 Dresden, Germany

- West '13 Visitor Registration is now open.
  - The last day for FREE Expo Only badge (a $150 onsite value) is May 10.
  - Register today!
  - www.semiconwest.org
- Technical Ballot Critical Dates
  - Cycle 3, 2013
    - Ballot Submission Date: April 17
    - Voting Period Starts: May 1
    - Voting Period Ends: May 31
  - Cycle 4, 2013
    - Ballot Submission Date: May 20
    - Voting Period Starts: June 1
    - Voting Period Ends: July 1
- Major Items Included in Revision to the Regulations
  - This revision to the Regulations added a new category called Complementary File.
    - TC Chapters must take action on Standards that reference files in formats other than pdf (e.g., XML schema, WDSL, xls)
    - All non-pdf files published prior to March 2013 Regulations are Various Materials.
    - TC Chapters must decide if non-pdf files are required for implementation of the Standard, and if so, TC Chapter must issue a ballot to make the non-pdf files "Complementary Files".
  - Elimination of Regional Standards
  - Exit mechanism from LOA in limbo
  - Clarification and additional guidance on Letter of Intent (LOI)
- March 2013 Publication Cycle
    - New Standards: 0
    - Revised Standards: 3
    - Reapproved Standards: 2
    - Withdrawn Standards: 0
    - Total SEMI Standards in portfolio: 871 (Includes 93 Inactive Standards)
- Standards Usage Interview
    - Looking for details on how standards are actually used:
    - Development/Engineering
    - Procurement
    - Manufacturing
    - Interview should take less than 30 minutes – contact James or any Standards staff
- The Official SEMI Standards Group
    - http://www.linkedin.com/groups/Official-SEMI-Standards-Group-1774298/about

Attachment – 4, SEMI Staff Report (Spring 2013) revB

6.0 Regulations Changes Report

6.1 See section 5 Staff Report above for new Regulations changes or check the latest version at www.semi.org/standards for additional information.

6.2 On the side note, Dinesh Gupta drew attention on the current SEMI Procedure Guide, section 2.5.1.1, which reads "*The author or TF leader should provide all of their TF members with a copy of the Draft for review and feedback for a week before it is submitted to Standards staff for Letter Ballot preparation.*" He stated that it is not possible to send the draft ballot to ALL task force members since not all TF leader keeps emails of all of their members. In effort to correct this section, he plans to participate in the SEMI Regulations subcommittee so he could propose a revision.
James Swirhun mentioned there are lots of email programs out there allowing one to manage an email group. If one wishes to opt out the email group, one can simply click for opting out. James recommended TF leaders to look into it.

7.0 Ballot Review

7.1 Document 5450A, Revision to SEMI M49-0912, Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 22 nm Technology Generations with Title Change to: Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations

7.1.1 Document passed technical review as balloted and was forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 5, 5450AProceduralReview

7.2 Document 5559, New Auxiliary Information: Interlaboratory Evaluation Of Nondestructive Method For Measuring The Edge Contour Of Silicon Wafers

7.2.1 Document was approved by the technical committee and was forwarded to the ISC Audits and Reviews Subcommittee for procedural review. See attachment below for detail of ballot adjudication.

Attachment – 6, 5559ProceduralReview

8.0 Task Force Reports

8.1 Specifications Group

8.1.1 Int'l 450 mm Wafer TF/Mike Goldstein (Intel)

Mike Goldstein reported the followings:

- The TF address in this meeting the G450C decision to test the notch free option.
- There was a lot of interest from the industry with 20 representatives attending the meeting.
- Pinyen Lin (450GC) presented the background for the consortium decision.
- There are already several ideas on potential fiducial designs (presentations attached).
  - From G450C
  - From KT
  - From Intel

See attachment below for all presentations.

Attachment – 7, International 450mm wafer TF report Spring 2013

8.1.2 Int'l Epitaxial Wafer TF/ Dinesh Gupta (STA)

Dinesh discussed a SNARF for doc. 5542, Line Items Revision to M62-0912, Specifications for Silicon Epitaxial Wafers, which was approved at SEMICON Japan.

8.1.3 Int'l Annealed Wafer TF/Dinesh Gupta (STA)

Dinesh Gupta reported doc. 5252A, Revision of SEMI M57-1011 with Title Change To: Specifications for Silicon Annealed Wafers, that was approved at Japan meeting. However, additional change needs to be made on M57. A new SNARF was submitted to revise M57.

Motion: To approve a SNARF for Revision of M57

By / 2nd: Jaydeep Sinha (KLA-Tencor)/George Kren (KLA-Tencor)
Discussion: None
Vote: 6/0. Motion passed

Attachment – 8, SNARF Rev To M57 040113

8.1.4 Int'l SOI TF/Mariam Sadaka (SOITEC USA)

Dinesh Gupta reported.

- Revision of SEMI M41-0707 Specification of Silicon-on-Insulator (SOI) for Power Device/ICs, needs to be submitted for cycle 4 ballot for review in San Francisco.

  Motion: To authorize doc. 5541, Revision of SEMI M41-0707 Specification of Silicon-on-Insulator (SOI) for Power Device/ICs, for cycle 4 ballot

  By / 2nd: Tetsuya Nakai (SUMCO)/Jaydeep Sinha (KLA-Tencor)
  Discussion: None
  Vote: 7/0. Motion passed

- The TF is discussing with the MEMS committee for their SOI wafer needs. It was reported that two types of bonded SOI thickness in pursued are >2um and ~1 um. The TF will try to reach out to companies in the US working on bonded SOI and invite them to participate in SEMI Standards.

Attachment – 9, SOI Meeting notes and update to the Si Wafer committee

8.1.5 Int'l Polished Wafer TF/Murray Bullis (Materials & Metrology)

Murray reported SNARF for doc. 5543, Line Items Revision of SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers, needs to be revised to allow additional line item change.
Motion: To approve revised SNARF 5543, Line Items Revision of SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers

By / 2nd: Murray Bullis (Materials & Metrology)/James Swirhun (Sinton Instruments)
Discussion: None
Vote: 7/0. Motion passed

Motion: To authorize ballot 5543, Line Items Revision of SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers, for cycle 4.

By / 2nd: Murray Bullis (Materials & Metrology)/Mike Goldstein (Intel)
Discussion: The text of the ballot was reviewed by the committee as James Swirhun disagreed with the line item 4 in ballot that was shown. He felt TF members should be given a chance to weight in as per SEMI Procedure Guide suggests that the ballot draft should be submitted to the TF members 7 days prior to submitting to SEMI for ballot submission. Shimizu-san also commented that he would only in favor of the motion with one a condition that the draft be sent to all members prior to ballot submission to SEMI. The motion was revised as following:
Revised motion: To approve authorize ballot 5543, Line Items Revision of SEMI M1-0413, Specifications for Polished Single Crystal Silicon Wafers, for cycle 4 with a condition that the TF members are in agreement with the ballot.

Vote: 7/0. Motion passed

In addition, the TF also discussed doc. 5500 New Standard: Specification for Polished Single Crystal Silicon Wafers for GaN-on-Silicon Applications, briefly and decided to plan a series of teleconferences between now and SEMICON® West to agree on a proper text for this document.

See attachment below for SNARF and other materials.
Attachment – 10, reinternationalpolishedwafertfmeeting

8.2 Metrology Group

8.2.1 Int'l Advanced Wafer Geometry TF/Jaydeep Sinha (KLA-Tencor)

Minutes were presented by Jaydeep Sinha. Highlights:

- Ballots
  - Doc. 5450A, Revision to SEMI M49, Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations
    - Passed and being forwarded to the ISC Audits & Reviews Subc for procedural review
  - Doc. 5430A, Revision to SEMI M73-0309, Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles
    - Will be reviewed at SEMICON West
- Ballot Development
  - Document 5343, Revision to SEMI M49-1011, Guide for Specifying Geometry Measurement Systems For Silicon: NT and ZDD scaling from reference wafer. Presentation from KLA-Tencor was made in response to scaling. There are several documents (M49, NT, and ZDD) that are linked with this issue and needs a clear SNARF for submission at SEMICON West
  - Aligning ITRS with AWG regarding proposed values
    - Mike Goldstein noted that Mike Walden is no longer participating in the ITRS. He asked the committee for a preventative to be involved.
    - Mike mentioned the 450 mm wafers geometry parameters are pulled back compared to ITRS's stringent value. The next ITRS meeting will be in April, which he plans to attend.
  - Doc. 5503, Revision to SEMI MF1390, Test Method for Measuring Warp on Silicon Wafers by Automated Non-Contact Scanning, to add bow measurement.
    - Noel brought up the need to define Bow in SEMI standard MF534 (Test Method for Bow of Silicon Wafers) seemed to be impractical for automated measurement and does not adequately define bow. He plans to circulate the draft among AWG TF members for comment. The document will be discussed at SEMICON West.
- New Business
  - Edge exclusion proposal G450C: by KwangWook Lee, G450C.
    - Mr. Lee had a proposal to extent FQA radius by another 0.5 mm (from 223 mm radius to 223.5 mm radius). This was primarily driven by Yield. A SNARF will be brought up at SEMI West by the G450C team.
- The AWG TF is planning a workshop on 450 mm Wafer to be held at SEMICON West on Wednesday, July 10, 2013. Tentative technical presentations include:
  - Towards 450 mm Silicon Wafer - M. Goldstein (Intel)
  - Edge Exclusion Proposal - K. Lee (Samsung/450GC)
  - 450 mm Notchless Wafer - P. Lin (TSMC/450GC)
  - Evolution of Wafer Geometry for Advanced Nodes - J. Sinha (KLA-Tencor)
  - Additional speakers from the Silicon Suppliers, IC Fab, and Equipment Manufacturers are being solicited. For question, please contact Jaydeep Sinha at Jaydeep.Sinha@kla-tencor.com or Kevin Nguyen at knguyen@semi.org

Attachment -11, AWG20130402

8.2.2 Int'l Advanced Surface Inspection TF/George Kren (KLA-Tencor)

George Kren discussed an old business with M52-0912 Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm to 11 nm Technology Generations, in table 1.13 "Less than 1% of adders allowed to contain metal". He mentioned that this would not be provable, and he will discuss with Fritz Passek (Siltronic) to come up with an agreeable line item change on M52 at the next meeting.

8.3 Committee Task Forces

8.3.1 Int'l Test Methods TF/Dinesh Gupta (STA)

Dinesh reported that the TF had two presentations given by Murray Bullis and James Swirhun on carrier lifetime. The TF has not come into an agreement with Doc. 5313B, Line Item Revisions of SEMI MF1535-0707, Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance. He reported the TF is continuing to work on MF1535. The discussion is resumed to the SEMICON West meeting.

Attachment -12, Intro to Carrier Recombination Lifetime Meas in Electronic Grade Si

Attachment -13, MF-1535 Technical Discussion

8.3.2 Int'l Terminology TF/Murray Bullis (Materials and Metrology)

No meeting. The next meeting is planned for SEMICON West.

9.0 Old Business

5 Year Review. The following documents are overdue for 5 year review.

- SEMI M35-1107, Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection
  - M35 should be reviewed by Int'l ASI TF. **Action Item** 1 – Kevin will email George Kren for discussion at their next TF meeting
- All these standards below are in need of leaders. Revisions are pending.
  - SEMI MF1723-1104, Practice for Evaluation of Polycrystalline Silicon Rods by Float-Zone Crystal Growth and Spectroscopy
  - SEMI MF1724-1104, Test Method for Measuring Surface Metal Contamination of Polycrystalline Silicon by Acid Extraction-Atomic Absorption Spectroscopy
  - SEMI MF1708-1104, Practice for Evaluation of Granular Polysilicon by Melter-Zoner Spectroscopies

10.0 New Business

10.1 JEITA Samples

Kevin reported that round robins samples from NIST were given to SEMI a few years ago. When Jim Erhstein (NIST) retired, these samples were sent to SEMI. JEITA samples were also part of the transfer. Now JEITA is requesting these samples to be transferred to AIST. The NA Silicon Wafer committee agreed to allow JEITA samples to be transferred to AIST. **Action Item 2** - Kevin will forward these samples to SEMI Japan staff to accommodate this request.

11.0 Action Item Reviews

Kevin Nguyen reviewed the old action items. There were two new actions items at this meeting noted in **table 7**.

12.0 Adjourn

The meeting was adjourned at 4:00 PM.

These minutes are respectfully submitted by:

Kevin Nguyen,
SEMI NA Standards Committee Manager
Phone: 408-943-7997
Email: knguyen@semi.org

Minutes approved by:

Noel Poduje (SMS) – Co-chair Date:

Dinesh Gupta (STA) – Co-chair Date: April 22, 2013

Table 8 – Index of Attachment Summary

#	*Title*	#	*Title*
1	Minutes NA SiWfr 20121030	8	SNARF Rev To M57 040113
2	EU Si Wafer liaison report_March 2013	9	SOI Meeting notes and update to the Si Wafer committee
3	JP_SiW_NA Spring_R0.1	10	reinternationalpolishedwafertfmeeting
4	SEMI Staff Report (Spring 2013) revB	11	AWG20130402
5	5450AProceduralReview	12	Intro to Carrier Recombination Lifetime Meas in Electronic Grade Si
6	5559ProceduralReview	13	MF-1535 Technical Discussion
7	International 450mm wafer TF report Spring 2013		

#1 Due to file size and delivery issues, attachments must be downloaded separately. A .zip file containing all attachments for these minutes is available at www.semi.org. For additional information or to obtain individual attachments, please contact Kevin Nguyen at the contact information above