Background Statement for SEMI Draft Document 5989

REVISION OF SEMI M62-0515, SPECIFICATION~~S~~ FOR SILICON EPITAXIAL WAFERS

Notice: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this Document.

Notice: Recipients of this Document are invited to submit, with their comments, notification of any relevant patented technology or copyrighted items of which they are aware and to provide supporting documentation. In this context, "patented technology" is defined as technology for which a patent has issued or has been applied for. In the latter case, only publicly available information on the contents of the patent application is to be provided.

Background

The Int'l Epitaxial Wafer TF issued line item ballot last year to correct nonconforming title of this standard as permitted in accordance with the Special Procedure listed in section A4-1 and Table A4-1 of the SEMI *Procedure Manual*. However, a reject was submitted on the scope section and the ballot failed. This new ballot has the following revisions:

a) Correct the title of this standard from "Specifications" to "Specification"

b) Delete 2.2 EDI codes no longer listed in M18

c) Delete 2.1.2.4 that is duplicate of 2.1.1.3

Notice: Additions are indicated by underline and deletions are indicated by ~~strikethrough~~.

Review and Adjudication Information

	Task Force Review	Committee Adjudication
Group:	Int'l Epitaxial Wafer TF	Silicon Wafer NA TC Chapter
Date:	July 11, 2016	July 12, 2016
Time & Timezone:	10:00AM – 12:00N PST	9:00AM – 12:00N PST
Location:	San Francisco, CA USA	San Francisco, CA USA
Leader(s):	Dinesh Gupta (STA) Naohisa Toda (Shinetsu Handotai)	Dinesh Gupta [dgupta@pacbell.net] Noel Poduje [noelp1@comcast.net]
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This meeting's details are subject to change, and additional review sessions may be scheduled if necessary. Contact the task force leaders or Standards staff for confirmation.

Telephone and web information will be distributed to interested parties as the meeting date approaches. If you will not be able to attend these meetings in person but would like to participate by telephone/web, please contact Standards staff.

Check www.semi.org/standards on calendar of event for the latest meeting schedule.

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LETTER BALLOT

SEMI Draft Document 5989

REVISION OF SEMI M62-0515, SPECIFICATIONS FOR SILICON EPITAXIAL WAFERS

Notice: Additions are indicated by underline and deletions are indicated by ~~strikethrough~~.

1 Purpose

1.1 Epitaxial silicon wafers are utilized for many integrated circuits and discrete semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the dimensions of epitaxial wafers to be standardized.

1.2 In addition, as technology advances to smaller and smaller dimensions for the elements of high density integrated circuits, it has become of interest to standardize additional properties of epitaxial wafers.

1.3 This Specification ~~These specifications~~ defines and provides examples of silicon epitaxial wafer requirements for both discrete semiconductor device manufacture and integrated circuit device manufacture. By defining inspection procedures and acceptance criteria, both suppliers and their customers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This Specification ~~These specifications~~ covers characteristics of both the substrate (through reference to SEMI M1) and the epitaxial layer, including handling and packaging.

2.1.1 The specification for epitaxial silicon wafers for discrete semiconductor device manufacture is specifically directed to silicon homoepitaxial deposits thicker than 25 µm on homogeneous silicon substrates or similar epitaxial wafers that are to be used to make discrete devices. For these wafers, device feature sizes are generally in excess of 1 µm.

2.1.1.1 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.1.1.2 Specific requirements for density of selected surface defects and variations of layer thickness and layer net carrier density are included together with AQLs for these properties.

2.1.1.3 In addition, Part 3 of the Silicon Wafer Specification Format for Order Entry,[1] which is included as Table 1, can be used to facilitate inclusion of such additional physical properties and suitable test methods as may be required in the specification.

2.1.2 The specifications for epitaxial silicon wafers for integrated circuit applications are restricted to wafers of diameter of 100 mm or greater with epitaxial layer thickness less than or equal to 25 µm.

2.1.2.1 This Specification ~~These specifications are~~ is specifically directed to silicon homoepitaxial deposits on homogeneous silicon substrates only, for which more stringent uniformity and surface defect criteria are required than for epitaxial silicon wafers for discrete semiconductor applications.

2.1.2.2 The primary standardized properties set forth in this ~~specification~~ Specification relate to physical, electrical, and surface defect parameters.

2.1.2.3 Specific requirements for density of selected surface defects (Table 2) and variations of layer thickness and layer net carrier density are included together with AQLs for these properties. One type of such defect is localized light scatterers (LLS) such as particles, pits, and other surface defects. A table of equivalent LLS density per unit area and number of LLS within the fixed quality area of a wafer is provided in Related Information 1.

~~2.1.2.4 In addition, Part 3 of the Silicon Wafer Specification Format for Order Entry, which is included as Table 1, can be used to facilitate inclusion of such additional physical properties and suitable test methods as may be required in the specification.~~

[1] This table was formerly included in SEMI M18.

2.1.2.5 Guides formed by a consensus of viewpoints are provided to suggest a foundation to specify an epitaxial wafer for use in integrated circuit manufacture at advanced design rules. Because these guides are not formal specifications but are suggestions from which a specification can evolve, they are provided in Related Information 2. The required specification is determined by the device and the process design. The usefulness of the guides can be increased by considering them prior to developing a device design or process.

2.2 ~~The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including epitaxial wafers, remains in SEMI M18.~~

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification~~s~~ for Polished Single Crystal Silicon Wafers

SEMI M17 — Guide for a Universal Wafer Grid

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide for Conversion Factors for Interstitial Oxygen in Silicon

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Reference Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M59 — Terminology for Silicon Technology

SEMI M78 — Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-Implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavenumber or Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant or Carrier Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and EPI Substrates by Secondary Ion Mass Spectrometry

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standards*[2]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Bar Code Label Standard

3.3 *DIN Standards*[3]

DIN 50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

DIN 50436 — Measurement of the Metallurgical Thickness of Epitaxial Layers of Silicon by the Stacking Fault Method

DIN 50437 — Measuring the Thickness of Silicon Epitaxial Layers by Infrared Interference Method

DIN 50439 — Determination of the Dopant Concentration Profile of Single Crystalline Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact

DIN 50441-3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

DIN 50443-1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-ray Topography: Silicon

DIN 50444 — Conversion between Resistivity and Dopant Density; Silicon

DIN 50447 — Contactless Determination of the Electrical Sheet Resistance of Semiconductor Layers with the Eddy-current Method

3.4 *European Community Directive*[4]

2002/95/EC — On the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment

3.5 *ISO Standards*[5]

ISO 14644-1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Airborne Particulates

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[2] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: 212.642.4900, Fax: 212.398.0023, http://www.ansi.org

[3] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

[4] *Official Journal of the European Union*, February 13, 2003 Available for downloading from the following URL: http://164.36.164.20/sustainability/pdfs/finalrohs.pdf

[5] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF) on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy (TXRF)

3.6 *JEITA Standard*[6]

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

3.7 *JIS Standards*[7]

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, acronyms, and symbols relating to silicon technology and epitaxial silicon technology are defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for epitaxial silicon wafers furnished to these specifications shall include the appropriate order entry information from Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, Table 1 in SEMI M1.

5.1.1 All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary flat length (or none)
- 2-6.5 Secondary flat location (or none)
- 2-6.6 Edge Profile
- 2-6.7 Thickness

5.1.2 Other items from Part 2, Polished Wafer or Substrate, can be included as needed.

5.1.3 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

[6] Formerly JEIDA 43; Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

[7] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

5.2 Purchase orders furnished to these specifications shall also include the items with a ♦ symbol in the left-most column of Table 1, Silicon Wafer Specification Format for Order Entry, Part 3. These are:

- 3-1.1 Conductivity Type/Structure
- 3-1.2 Layer Dopant
- 3-1.3 Silicon Source Gas
- 3-1.4 Layer Growth Method
- 3-1.5 Layer Net Carrier Density or Resistivity, center point
- 3-1.6 Net Carrier Density Variation
- 3-1.7 Layer Thickness, center point
- 3-1.8 Layer Thickness Variation

NOTE 1: The dopant, doping method, and growth method are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics should be agreed upon between the supplier and the customer (see § 9).

NOTE 2: Care should be taken in converting between carrier density and resistivity using SEMI MF723. Multiple conversions may introduce differences in values. For example, converting from carrier density (C_i) to resistivity and back to carrier density (C_f), may result in C_i not equaling C_f.

5.2.1 Also, appropriate epitaxial wafer defect limits from 3-4 and 3-5 of Part 3 shall be included. The importance of various defects may vary from application to application, but minimum requirements for defect limits for epitaxial wafers are given in Table 2.

5.2.2 Limits for slip, which may require destructive testing, shall be specified in the purchase order together with an appropriate test method.

5.2.3 Other items from Part 3, Epitaxial Wafer, can be included as needed.

5.2.4 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures.

5.3.2 Certification (if required).

5.3.3 Packing and shipping container labeling requirements.

6 Requirements

6.1 As a minimum, the substrate shall conform to SEMI M1 and the appropriate substrate (polished wafer) category requirements (see Tables 5 through 11 in SEMI M1 for the requirements for various wafer categories).

6.2 If specified on the purchase order, the wafers shall conform to the Restriction of Hazardous Substances (RoHS) regulatory requirements of EC Directive 2002/95/EC. For information, the maximum concentrations of Cr, Cd, Hg, and Pb in the bulk or on the surface of the wafer required by this directive are given in SEMI M1.

6.3 Epitaxial wafer defects shall not exceed the limits given in Table 2. In this table, the defect limits (except for edge chips and indents) apply to the fixed quality area of the wafer except for any area included in a window where there is a laser identification mark.

6.3.1 In the absence of another specification, epitaxial wafers for IC applications shall contain no slip lines within the quality area.

NOTE 3: When an unetched wafer is observed for slip it is impossible to differentiate between slip and linear misfit lines.

6.4 *Layer Thickness Variation*

6.4.1 *Epitaxial Wafer for Discrete Semiconductor Device Manufacture* — Unless otherwise specified, the thickness variation shall be determined from values measured at the center and half radius ($R/2$) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤6% defined as follows:

$$\text{Variation (\%)} = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \tag{1}$$

where $\frac{R}{2}$ denotes one of the thickness values measured at half radius and C denotes the value at the center.

6.4.2 *Epitaxial Wafer for IC Applications* — Unless otherwise specified, the thickness variation shall be determined from value measured at the center and locations centered 12 mm ± 1 mm from the periphery, on diameters both parallel and perpendicular to the primary flat or notch axis, as follows:

$$\text{Variation (\%)} = \frac{t_{\max} - t_{\min}}{t_{\max} + t_{\min}} \times 100 \tag{2}$$

where $t_{\max}$ and $t_{\min}$ denote the maximum and minimum thickness values measured. The 12 mm locations have been defined based on instrument processing and fixturing considerations.

6.5 *Layer Net Carrier Density Variation*

NOTE 4: In many cases, this variation is described in terms of resistivity variation. It is possible to convert between resistivity and net carrier density with the use of SEMI MF723. However, it must be noted that the center point of a specification expressed in resistivity differs from that expressed in net carrier density. Consequently, the distributions may be skewed in different ways around the center point.

6.5.1 *Epitaxial Wafer for Discrete Semiconductor Device Manufacture* — The net carrier density variation shall be determined from values measured at the center and half radius ($R/2$) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤10% for net carrier density ≥1×10^{15} cm^{-3} and ≤15% for net carrier density <1×10^{15} cm^{-3} defined as follows:

$$\text{Variation (\%)} = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \tag{3}$$

where $\frac{R}{2}$ denotes one of the net carrier density values measured at half radius and C denotes the value at the center.

Table 1 Silicon Wafer Specification Format for Order Entry, Part 3 Epitaxial Wafer

		ITEM	*SPECIFICATION*	*MEASUREMENT METHOD*
3-1. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify an epitaxial silicon wafer.)*				
		FOR EPITAXIAL WAFERS FOR IC APPLICATIONS, THE ITEMS LISTED IN THIS ENTIRE TABLE MAY BE SPECIFIED INDIVIDUALLY OR [ ]Specified according to Epitaxial Wafer Category 11.[ ] (see Tables R2-1 through R2-4 for epitaxial wafer categories). If the items are specified according to a standard category, none need be entered individually anywhere in this table unless (1) a choice must be made between various options in the category requirements or (2) an exception is desired.		
♦	3-1.1	Conductivity Type/Structure	[ ]n/n^+; [ ]p/p^-; [ ]p/p^+; [ ]p/p^{++}; [ ]Other: (specify)_____	
♦	3-1.2	Layer Dopant	[ ]Boron; [ ]Phosphorus; [ ]Arsenic	
♦	3-1.3	Silicon Source Gas	[ ]SiH_4; [ ]SiH_2Cl_2; [ ]$SiHCl_3$; [ ]$SiCl_4$;	
♦	3-1.4	Layer Growth Method	Reactor Type [ ]; Pressure [ ]	

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
♦	3-1.5	Layer Net Carrier Density or Resistivity, center point If Resistivity is Measured Convert to Net Carrier Density	Nominal [ ] ± Tolerance [ ] × $10^{[\ ]}$ atoms/cm^3 or Nominal [ ] ± Tolerance [ ] Ω·cm [ ]Yes; [ ]No	[ ]SEMI MF1392; [ ]DIN 50439; [ ]SEMI MF398; [ ]SEMI MF374; [ ]SEMI MF672; [ ]DIN 50447 [ ]Other: (specify)_____ [ ]SEMI MF723 [ ]DIN50444
♦	3-1.6	Net Carrier Density Variation Measurement Position and Calculation	[ ]≤10%; [ ]≤15%; [ ]≤____% [ ]Center and Half Radius (Equation 3); [ ]Center and 12 mm from edge (Equation 4); [ ]Other_____	[ ]SEMI MF1392; [ ]DIN 50439, [ ]Other: (specify)_____
♦	3-1.7	Layer Thickness, center point	Nominal [ ] ±Tolerance [ ] µm	[ ]SEMI MF95; [ ]DIN 50437; [ ]SEMI MF110; [ ]SEMI MF672; [ ]DIN 50436; [ ]Other: (specify)_____
♦	3-1.8	Layer Thickness Variation Measurement Position and Calculation	[ ]≤6%; [ ]≤____% [ ]Center and Half Radius (Equation 1); [ ]Center and 12 mm from edge (Equation 2); [ ]Other_____	Use same method as in 3-1.7 at each position
	3-1.9	Transition Width	[ ]≤_____µm	Use same methods as in 3-1.7 (IR only, for thickness measurement) and 3-1.10 (for carrier density measurement)
	3-1.10	Flat Zone	[ ]≤_____µm	[ ]SEMI MF1392; [ ]DIN 50439; [ ]Other: (specify)_____
	3-1.11	Phantom Layer	[ ]None	
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
	3-2.1	Bow	[ ]≤_____ µm	[ ]JIS H 0611; [ ]Other: (specify)_____
	3-2.2	Warp	[ ]≤_____ µm	[ ]SEMI MF1390; [ ]Other: (specify)_____
	3-2.3	Sori	[ ]≤_____ µm	[ ]SEMI MF1451; [ ]Other: (specify)_____
	3-2.4	Total Thickness Variation	[ ]TTV; [ ]GBIR; [ ]Other: (specify)_____	[ ]SEMI MF533; [ ]SEMI MF1530; [ ]JIS H 0611; [ ]DIN 50441/1; [ ]Other: (specify)_____
	3-2.5	Flatness, Global	[ ]≤_____ µm; Acronym[#1] [ ] [ ] [ ] [ ]	[ ]SEMI MF1530; [ ]DIN 50441/3; [ ]JEITA EM-3401; [ ]Other: (specify)_____
	3-2.6	Flatness, Site	[ ]≤_____ µm; Acronym[#1] [ ] [ ] [ ] [ ] Site Size ___ mm × ___ mm [ ]% Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: *x* = [ ] mm, *y* = [ ] mm	[ ]SEMI MF1530; [ ]Other: (specify)_____
	3-2.7	Nanotopography	[ ]≤___ nm for 2 mm diameter analysis area; and [ ]≤___ nm for 10 mm diameter analysis area; [ ]Other: (specify) _____	[ ]SEMI M43; [ ]Other: (specify)_____
	3-2.8	Misfit dislocations	[ ]to be determined	[ ]to be determined
	3-2.9	Flatness, Site, SBIR	[ ]to be determined	[ ]SEMI MF1530; [ ]Other: (specify)_____
	3-2.10	Edge Profile	[ ]to be determined	[ ]to be determined
	3-2.11	Edge Roll Off	[ ]to be determined	[ ]to be determined

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		ITEM	*SPECIFICATION*	*MEASUREMENT METHOD*
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
	3-3.1	Surface Metal Contamination		
	3-3.1.1	Sodium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	3-3.1.2	Aluminum	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	3-3.1.3	Potassium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.4	Chromium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.5	Iron	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.6	Nickel	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.7	Copper	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.8	Zinc	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.1.9	Calcium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2	Other Surface Metals (List Separately)		
	3-3.2.1	Cobalt	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.2	Manganese	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____

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	ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
	3-3.2.3	Molybdenum	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.4	Titanium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.5	Vanadium	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	3-3.2.6	[ ]Other: (specify)_____	[ ]≤[ ] × 10[ ]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
	THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE: [ ]Specified according to Table 2, Discrete Applications, or [ ]Specified according to Table 2, IC Applications. In either of these latter cases, individual listed items need not be entered individually in this section unless an exception is desired.			
	3-4.1	Stacking Faults	[ ]1/cm^2; [ ]Other: (specify)_____	[ ]SEMI MF1726; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.2	Slip	[ ]36 grid elements (Discrete Epitaxial Wafer only); [ ]None; [ ]Other: (specify)_____	[ ]SEMI M17 [ ]SEMI MF1726
	3-4.3	Dislocations	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF1726
	3-4.4	Large Localized Light Scatterers, Size >1 µm on side	[ ]None; Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.5	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.6	Haze	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.7	Scratches – Macro	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.8	Scratches – Micro	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____

	ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
	3-4.9	Edge Chips and Indents	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.10	Foreign Matter	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.11	Dimples	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.12	Orange Peel	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.13	Contamination/Area	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.14	Edge Cracks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.15	Edge Crown	[ ]Projection above layer surface ≤1/3 of layer thickness; [ ]None; [ ]Other: (specify)_____	[ ]DIN 50446; [ ]Other: (specify)_____
	3-4.16	Cracks, Crow's Feet	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.17	Mounds	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.18	Saw Marks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-4.19	Dopant Striation Rings	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]DIN 50443/1; [ ]Other: (specify)_____
	3-4.20	Stains	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
	THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE [ ]Specified according to Table 2, Discrete Applications, or [ ]Specified according to Table 2, IC Applications. In either of these latter cases, individual listed items need not be entered individually in this section unless an exception is desired.			
	3-5.1	Contamination	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
	3-5.2	Scratches – Macro	[ ]None; [ ]Other: (specify cum length)_____ mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-5.3	Scratches – Micro	[ ]None; [ ]Other: (specify cum length)_____ mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____
	3-5.4	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#2] [ ]Other: (specify)_____

	ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
	3-5.5	Edge Chips	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.6	Cracks, Crow's Feet	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.7	Saw Marks	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;#2 [ ]Other: (specify)_____
	3-5.8	Stains	[ ]None; [ ] Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]Other: (specify)_____
3-6. OTHER POST-EPI CHARACTERISTICS (as required)				

#1 Flatness Acronyms are defined in the Flatness Decision Tree in Appendix 1 of SEMI M1.

#2 In today's technology, it may be possible to inspect for some of these items using automated surface scanning inspection systems (SSIS). Such systems should be calibrated according to SEMI M53 using polystyrene latex spheres deposited in accordance with SEMI M58. Some indication of the defects separable by such instruments is provided in SEMI M35; however, a standard test procedure has yet to be developed. Application of automated inspection with the use of an SSIS must be agreed upon between supplier and customer.

Table 2 Epitaxial Wafer Defect Limits

Item	*Characteristic*	*Maximum Limit*#1				
		Discrete Applications				*IC Applications*
		$t_{epi} < 25\ \mu m$	$50 > t_{epi} \geq 25\ \mu m$	$100 > t_{epi} \geq 50\ \mu m$	$t_{epi} \geq 100\ \mu m$	
3-4.1	Stacking Faults	15 per cm^2				1 per cm^2
3-4.2	Slip	n = 36 grid elements (SEMI M17)				None
3-4.3	Dislocations	not specified				None
3-4.4	Large LLS, at ≥20 µm LSE	0.07 per cm^2	0.09 per cm^2	0.12 per cm^2	0.15 per cm^2	Not specified
3-4.5	Total LLS, at ≥0.5 µm LSE	0.20 per cm^2	0.24 per cm^2	0.27 per cm^2	0.30 per cm^2	0.20 per cm^2
3-4.6	Haze#2	None				None
3-4.7	Scratches – Macro#3	None				None
3-4.8	Scratches – Micro#3	None				None
3-4.9	Edge Chips and Indents#4	None				None
3-4.10	Foreign Matter#2	None				None
3-4.15	Edge Crown#5	Projection above wafer surface not to exceed $(1/3)t_{epi}$				Not specified
3-5.1	Back Surface Contamination#2	None				None

#1 Except for edge chips and indents, defect limits apply to the fixed quality area of the wafer except for any area included in a window where there is a laser identification mark. Nominal edge exclusion is 4 mm for 150 mm wafers, 4, 3, or 2 mm for 200 mm wafers, and 3, 2, or 1 mm for 300 mm wafers.

#2 Any adherent contaminants, such as stains, glove marks, dirt, smudges, warps, and solvent residues. This characteristic does not include point defects. Any nonadherent contamination or particulate matter easily removed by industry-accepted cleaning techniques shall not constitute foreign matter or haze.

#3 The cumulative AQL for both front surface and back surface of wafer is 2.5.

#4 The cumulative AQL for both front surface and back surface of wafer is 1.0.

#5 Edge crowning may be reduced by pre-epitaxy edge rounding or removed by post-epitaxy edge rounding.

6.5.2 *Epitaxial Wafer for IC Applications* — The net carrier density variation shall be determined from values measured at the center and locations with center of the probe at 12 mm ± 1 mm from the periphery, on diameters both parallel and perpendicular to the primary flat or notch axis, as follows:

$$\text{Variation}\,(\%) = \frac{N_{\max} - N_{\min}}{N_{\max} + N_{\min}} \times 100 \quad (4)$$

where N_{max} and N_{min} denote the maximum and minimum net carrier density values measured. The 12 mm locations have been defined based on instrument processing and fixturing considerations.

7 Specification Guides for IC Applications

7.1 Guides for specifying epitaxial wafers for IC applications are provided in Related Information 2. These guides cover epitaxial wafers for use in fabricating ICs with design rule of 1 µm or smaller. These guides provide a series of options intended to increase the awareness of epitaxial specifications and to provide information from which a specification can be formulated.

7.2 The information provided in the guides was formed by a consensus of viewpoints. The guides may or may not be used as a foundation to specify an epitaxial wafer for use in device manufacture. Their usefulness can be increased by considering the information in the appropriate guide prior to developing a device design or process. The required specification is determined by the device and the process design; the guides are suggestions from which a specification can evolve.

7.3 A specification guide can be viewed as a generic epitaxial wafer specification or as an example of a specification. These tables provide common epitaxial wafer characteristics which describe starting wafers useful for the manufacture of some twin tub CMOS devices. When suitable to the application, the guides can be used intact, reducing the proliferation of specifications and formats. Categories have been defined for epitaxial wafers that follow the specifications given in the specification guides. These are summarized in Table 3.

Table 3 Epitaxial Wafer Categories

Epitaxial Wafer Category	*Design Rule*	*Technology*
11.3	1.0 µm	Twin-Tub CMOS
11.4	0.35 µm	Twin-Tub CMOS
11.5	0.35 µm	DRAM
11.6	0.25 µm	Twin-Tub CMOS
11.7.1	0.18 µm	p/p^-, DRAM
11.7.2	0.18 µm	p/p^+, DRAM, Logic
11.7.3	0.18 µm	p/p^{++}, Logic
11.9.1	130 nm	p/p^-, DRAM
11.9.2	130 nm	p/p^+, DRAM, Logic
11.9.3	130 nm	p/p^{++}, Logic
11.10.1	90 nm	p/p^-, DRAM
11.10.2	90 nm	p/p^+, DRAM, Logic
11.10.3	90 nm	p/p^{++}, Logic
11.11.1	65 nm	p/p^-, DRAM
11.11.2	65 nm	p/p^+, DRAM, Logic
11.11.3	65 nm	p/p^{++}, Logic
11.12.1	45 nm	p/p^-, DRAM
11.12.2	45 nm	p/p^+, DRAM, Logic
11.12.3	45 nm	p/p^{++}, Logic
11.13.1	32 nm	p/p^-, DRAM
11.13.2	32 nm	p/p^+, DRAM, Logic
11.13.3	32 nm	p/p^{++}, Logic
11.14.1	22 nm	p/p^-, DRAM

Epitaxial Wafer Category	*Design Rule*	*Technology*
11.14.2	22 nm	p/p^+, DRAM, Logic
11.14.3	22 nm	p/p^{++}, Logic
11.15.1	16 nm	p/p^-, DRAM
11.15.2	16 nm	p/p^+, DRAM, Logic
11.15.3	16 nm	p/p^{++}, Logic

7.3.1 Table R2-1 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 1.0 µm, 0.35 µm, or 0.25 µm design rules.

7.3.1.1 The criteria for all three design rules are given for epitaxial wafers to be used for twin-tub CMOS devices, such as, but not limited to, ASICs, FPGAs, linears, DSPs, and microprocessors.

7.3.1.2 Typical criteria for 0.35 µm design rules are also given for epitaxial wafers to be used for devices such as 64 Mb DRAMs.

7.3.2 Table R2-2 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of twin tub CMOS, 0.18 µm design rule devices.

7.3.3 Table R2-3 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of twin tub CMOS, 130 nm design rule devices.

7.3.4 Table R2-4 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 90 nm design rule CMOS devices.

7.3.5 Table R2-5 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 65 nm design rule CMOS devices.

7.3.6 Table R2-6 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 45 nm design rule CMOS devices.

7.3.7 Table R2-7 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 32 nm design rule CMOS devices.

7.3.8 Table R2-8 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 22 nm design rule CMOS devices.

7.3.9 Table R2-9 gives typical epitaxial wafer criteria that can be used to develop a specification for wafers to be used in the fabrication of 16 nm design rule CMOS devices.

8 Sampling

8.1 Unless otherwise specified, appropriate sample sizes shall be selected from each lot according to ANSI/ASQ Z1.4-1993. Quality characteristics shall be assigned an acceptable quality level (AQL) in accordance with ANSI/ASQ Z1.4-1993. Inspection levels shall be agreed upon between supplier and customer. Accept and reject criteria are to be based on defective wafers, not on defective characteristics.

8.2 Unless otherwise specified, the following AQL's shall be assigned:

8.2.1 *Epitaxial Wafer for Discrete Semiconductor Device Manufacture*

- Epitaxial Layer Center-point Thickness and Variation, 6.5%;
- Epitaxial Layer Center Net Carrier Density and Variation, 6.5%;
- Epitaxial Wafer Defects, Cumulative, 4.0%.

8.2.2 *Epitaxial Wafer for IC Applications*

- Epitaxial Layer Center-point Thickness and Variation, 1%;
- Epitaxial Layer Center Net Carrier Density and Variation, 1%;

- Epitaxial Wafer Defects, Cumulative, 2.5%.

9 Test Methods

9.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, JIS, or DIN standard test methods for the item as selected from the Silicon Wafer Specification Format for Order Entry, Parts 2 and 3, located in Table 1 of SEMI M1 and Table 1 herein, respectively, and specified in the purchase order.

9.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

9.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

9.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

9.5 Information about various test methods appropriate to substrate and epitaxial wafer testing is provided in Related Information 2 of SEMI M1 together with information about some additional test methods no longer in wide use throughout the industry

9.6 *Test Methods for Properties of the Epitaxial Layer*

9.6.1 *Thickness* — In the case of thin layers and graded doping transitions, the methods cited in Item 3-1.7 (Table 1) are likely not to be suitable. See the scopes of these test methods to determine their limitations. In measuring transition width, only infrared techniques apply; these are given in SEMI MF95 and DIN 50437. In all cases, there is a possibility that various types of infrared reflectance instrumentation may result in different values of epitaxial layer thickness. Therefore, both the test method and the instrumentation used shall be agreed upon between supplier and customer.

9.6.2 *Net Carrier Density* — SEMI MF1392 and DIN 50439 are methods for measuring net carrier density using a mercury probe contact. If resistivity is measured, as by SEMI MF374, SEMI MF525, or DIN 50447, conversion to dopant density shall be made using SEMI MF723 or DIN 50444, which are technically equivalent. Net carrier density of very heavily doped layers (or substrates) may be found using SEMI MF398. Net carrier density profiles may be determined directly in accordance with SEMI MF1392 or DIN 50439 or indirectly in accordance with SEMI MF672, with conversion from resistivity to net carrier density in accordance with SEMI MF723 or DIN 50444. If the method used for determining the net carrier density profile is not the same as that used to determine the center-point net carrier density, correlation between the two methods used shall be established.

9.6.3 *Epitaxial Wafer Defects*

9.6.3.1 Surface inspection shall be performed before any other testing. Wafers may be cleaned prior to inspection to minimize difficulty in the visual inspection of defects other than foreign matter.

9.6.3.2 *Slip* — For observation of gross slip, examination of the epitaxial layer under the illumination conditions specified in ¶ 12.2 of SEMI MF523 may suffice. For more demanding applications, it may be desirable to etch the surface in accordance with SEMI MF1726 prior to the visual inspection.

9.6.3.3 Inspection for slip on epitaxial wafers intended for discrete device manufacture shall be done using grid elements constructed in accordance with SEMI M17. An element is defective if it contains one or more slip lines. The total number of elements shall be less than or equal to *n*, where *n* is listed in Table 2.

9.6.3.4 Automatic surface inspection technology is being developed to detect and discriminate surface defects. The use of SEMI M35 is intended to facilitate this development.

9.7 If substrates of different type and net carrier density than the product substrates are to be used for deposition control, their type, resistivity, and quantity per run or lot shall be agreed upon between supplier and customer.

10 Certification

10.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

10.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in § 9. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

11 Product Labeling

11.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one year after that particular lot has been accepted by the customer.

11.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶ 11.1 that is not included on the label shall be retained in the supplier's data base for at least one month after that particular lot has been accepted by the customer.

11.3 Epitaxial wafers of 300 mm diameter shall be shipped in packages labeled in accordance with SEMI M45.

12 Packing and Marking Shipping Container Labeling

12.1 Special packing requirements shall be subject to agreement between the supplier and customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

12.2 Epitaxial wafers of 300 mm diameter shall be shipped in accordance with SEMI M45.

12.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with ANSI/EIA 556-B.

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RELATED INFORMATION 1
LLS DENSITY EQUIVALENTS

NOTICE: This Related Information is not an official part of SEMI M62 and was derived from the work of the global Silicon Wafer Technical Committee. This Related Information was approved for publication by full letter ballot procedures on September 8, 2005.

R1-1 Introduction

R1-1.1 Table R1-1 gives the number of localized light scatterers in the fixed quality area of wafers of various nominal diameters and various values of nominal edge exclusion, *EE*, that is equivalent to the LLS density per cm^2 and LLS density per m^2 given in the first two columns.

Table R1-1 Number of Localized Light Scatterers in the Fixed Quality Area of Wafers of Different Sizes as a Function of LLS Density

LLS Density per cm^2	*LLS Density per m^2*	*Nominal Diameter, mm*										
		2 in.	*3 in.*	*100 mm*	*125 mm*	*150 mm*	*200 mm*			*300 mm*		
		EE=2 mm	*EE=2 mm*	*EE=3 mm*	*EE=3 mm*	*EE=4 mm*	*EE=4 mm*	*EE=3 mm*	*EE=2 mm*	*EE=3 mm*	*EE=2 mm*	*EE=1 mm*
0.01	100	0	0	0	1	1	2	2	3	6	6	6
0.02	200	0	0	1	2	3	5	5	6	13	13	13
0.03	300	0	1	2	3	4	8	8	9	20	20	20
0.04	400	0	1	2	4	6	11	11	12	27	27	27
0.05	500	0	2	3	5	7	14	14	15	33	34	34
0.06	600	1	2	4	6	9	17	17	18	40	41	41
0.07	700	1	2	4	7	11	20	20	21	47	48	48
0.08	800	1	3	5	8	12	23	23	24	54	55	55
0.09	900	1	3	6	10	14	26	26	27	61	61	62
0.10	1000	1	4	6	11	15	28	29	30	67	68	69
0.11	1100	1	4	7	12	17	31	32	33	74	75	76
0.12	1200	2	4	8	13	19	34	35	36	81	82	83
0.13	1300	2	5	9	14	20	37	38	39	88	89	90
0.14	1400	2	5	9	15	22	40	41	42	95	96	97
0.15	1500	2	6	10	16	23	43	44	45	101	103	104
0.16	1600	2	6	11	17	25	46	47	48	108	110	111
0.17	1700	2	6	11	18	26	49	50	51	115	116	118
0.18	1800	3	7	12	20	28	52	53	54	122	123	125
0.19	1900	3	7	13	21	30	55	56	57	128	130	132
0.20	2000	3	8	13	22	31	57	59	60	135	137	139
0.21	2100	3	8	14	23	33	60	62	63	142	144	146
0.22	2200	3	9	15	24	34	63	65	66	149	151	153
0.23	2300	3	9	15	25	36	66	67	69	156	158	160
0.24	2400	4	9	16	26	38	69	70	72	162	165	167
0.25	2500	4	10	17	27	39	72	73	75	169	172	174
0.26	2600	4	10	18	28	41	75	76	78	176	178	181
0.27	2700	4	11	18	30	42	78	79	81	183	185	188
0.28	2800	4	11	19	31	44	81	82	84	190	192	195

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LLS Density per cm^2	*LLS Density per m^2*	*Nominal Diameter, mm*										
		2 in.	*3 in.*	*100 mm*	*125 mm*	*150 mm*	*200 mm*			*300 mm*		
		EE=2 mm	*EE=2 mm*	*EE=3 mm*	*EE=3 mm*	*EE=4 mm*	*EE=4 mm*	*EE=3 mm*	*EE=2 mm*	*EE=3 mm*	*EE=2 mm*	*EE=1 mm*
0.29	2900	4	11	20	32	45	83	85	87	196	199	202
0.30	3000	5	12	20	33	47	86	88	90	203	206	209
0.31	3100	5	12	21	34	49	89	91	93	210	213	216
0.32	3200	5	13	22	35	50	92	94	96	217	220	223
0.33	3300	5	13	22	36	52	95	97	99	224	227	230
0.34	3400	5	13	23	37	53	98	100	102	230	233	237
0.35	3500	6	14	24	38	55	101	103	105	237	240	244
0.36	3600	6	14	24	40	57	104	106	108	244	247	251
0.37	3700	6	15	25	41	58	107	109	111	251	254	258
0.38	3800	6	15	26	42	60	110	112	114	257	261	265
0.39	3900	6	15	27	43	61	112	115	117	264	268	272
0.40	4000	6	16	27	44	63	115	118	120	271	275	278
0.41	4100	7	16	28	45	64	118	121	123	278	282	285
0.42	4200	7	17	29	46	66	121	124	126	285	289	292
0.43	4300	7	17	29	47	68	124	127	129	291	295	299
0.44	4400	7	18	30	48	69	127	130	132	298	302	306
0.45	4500	7	18	31	50	71	130	133	135	305	309	313
0.46	4600	7	18	31	51	72	133	135	138	312	316	320
0.47	4700	8	19	32	52	74	136	138	141	319	323	327
0.48	4800	8	19	33	53	76	138	141	144	325	330	334
0.49	4900	8	20	34	54	77	141	144	147	332	337	341
0.50	5000	8	20	34	55	79	144	147	150	339	344	348

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RELATED INFORMATION 2
GUIDES FOR SPECIFICATION OF EPITAXIAL WAFERS FOR IC APPLICATIONS

NOTICE: This Related Information is not an official part of SEMI M62 and was derived from the work of the global Silicon Wafer Technical Committee. This Related Information was approved for publication by full letter ballot procedures on January 2, 2009.

Table R2-2 Guide for Specification of 1.0 µm, 0.35 µm, and 0.25 µm Design Rule Epitaxial Wafers

Previous SEMI Reference:		*SEMI M11, Table 3*	*SEMI M11, Table 4*	*SEMI M11, Table 5*	*SEMI M11, Tables 6 and 8*
Design Rule:		*1.0 µm*	*0.35 µm*	*0.35 µm*	*0.25 µm*
Epitaxial Wafer Category:		*11.3*	*11.4*	*11.5*	*11.6*
Technology		*Twin-Tub CMOS*	*Twin-Tub CMOS*	*DRAM*	*Twin-Tub CMOS*
2. SUBSTRATE CHARACTERISTICS					
2-1.1	Growth Method	Supplier option of Cz or MCz			
2-1.3	Crystal Orientation	(100)			
2-1.4	Conductivity Type	p^+			
2-1.5	Dopant	Boron			
2-1.8	Wafer Surface Orientation	Off-orientation 0.6° ± 0.4°			
2-2.1	Resistivity, Center point[#1]	0.005–0.020 Ω·cm	0.005–0.010 Ω·cm	0.005–0.010 Ω·cm or 0.005–0.020 Ω·cm	0.005–0.010 Ω·cm or 0.005–0.020 Ω·cm
2-3.1	Oxygen Concentration[#2]			≤1.5 × 10^{18} cm^{-3} (≤30 ppma), old ASTM	
2-4.8	Bulk Micro Defects (BMD)	Not specified	Customer specified		
2-5.1	Wafer ID Marking			A/N, SEMI M13	SEMI M12, SEMI M13 or SEMI T1
2-5.3	Denuded Zone	Not specified	Customer specified		
2-5.4	Extrinsic gettering			Customer specified	
2-5.5	Backseal[#1,#3]	Required for 0.005–0.010 Ω·cm; Customer specified for 0.005–0.020 Ω·cm			
2-6.1	Nominal Diameter[#1]	150 mm, 200 mm, or 300 mm		200 mm only	150 mm or 200 mm
2-6.3	Flat, notch	Per SEMI M1, depending on category of wafer substrate		Notch only	Customer specified
2-6.8	Total Thickness Variation	Not specified		≤5 µm, GBIR	
2-6.10	Warp	Not specified		Customer specified	Not specified
2-6.12	Global Flatness	Not specified		≤3 µm, GFLR	Not specified
2-6.13	Site Flatness			≤0.35 µm SFQD 22 mm × 22 mm sites 95% Usable Area No partial sites	≤0.25 µm SFQR 22 mm × 22 mm sites Negotiated %UA Include partial sites
2-10.1	Inspection Sheet[#4]			Certificate Required in a standard format to be determined	
2-10.2	SQC Data Sheet[#4]			SQC Required in a standard format to be determined	

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Previous SEMI Reference:		*SEMI M11, Table 3*	*SEMI M11, Table 4*	*SEMI M11, Table 5*	*SEMI M11, Tables 6 and 8*
Design Rule:		*1.0 µm*	*0.35 µm*	*0.35 µm*	*0.25 µm*
Epitaxial Wafer Category:		*11.3*	*11.4*	*11.5*	*11.6*
Technology		*Twin-Tub CMOS*	*Twin-Tub CMOS*	*DRAM*	*Twin-Tub CMOS*
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS					
3-1.1	Conductivity Type/Structure	p/p^+			
3-1.2	Layer Dopant	Boron			
3-1.3	Silicon Source Gas	Fixed by agreement		Not specified	Fixed by agreement
3-1.4	Layer Growth Method	Fixed by agreement		Not specified	Fixed by agreement
3-1.5	Layer Net Carrier Density, center point[#5]	$2.00 \pm 1.0 \times 10^{15}$ carriers/cm^3	$2.00 \pm 0.5 \times 10^{15}$ carriers/cm^3	Target $\geq 1.34 \times 10^{15}$ carriers/cm^3 Tolerance ±25% (2σ) of Target	
3-1.6	Net Carrier Density Variation	10% max per Equation 4		±20% per Equation 4	10% max per Equation 4
3-1.7	Layer Thickness, center point	Target ±10%	Target ±5% (1σ)	≤5 µm ±5% (1σ)	2–5 µm ± 5% (1σ)
3-1.8	Layer Thickness Variation	10% max per Equation 2			
3-1.9	Transition Width			Customer specified	
3-1.11	Phantom Layer	None			
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS					
3-2.6	Flatness, Site	≤0.5 µm SFQD 18 mm × 18 mm sites 95% Usable Area Include partial sites No offset	≤0.23 µm SFQD 22 mm × 22 mm sites 95% Usable Area Include partial sites No offset		≤0.25 µm SFQR 22 mm × 22 mm sites Negotiated %UA Include partial sites No offset
3-3. POST-EPI FRONT SURFACE CHEMISTRY					
3-3.1.1	Sodium	$\leq 2 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.2	Aluminum	$\leq 1 \times 10^{12}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 2 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.4	Chromium	$\leq 2 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.5	Iron	$\leq 2 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.6	Nickel	$\leq 1 \times 10^{12}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.7	Copper	$\leq 2 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		$\leq 5 \times 10^{10}$ cm^{-2}
3-3.1.8	Zinc	$\leq 1 \times 10^{12}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.9	Calcium	Not specified			$\leq 5 \times 10^{10}$ cm^{-2}
3-3.2.1	Cobalt	Not specified			$\leq 5 \times 10^{10}$ cm^{-2}
3-3.2.2	Manganese	Not specified			$\leq 5 \times 10^{10}$ cm^{-2}
3-3.2.3	Molybdenum	Not specified			$\leq 5 \times 10^{10}$ cm^{-2}
3-3.2.4	Titanium	Not specified			$\leq 5 \times 10^{10}$ cm^{-2}
3-3.2.5	Vanadium	Not specified			$\leq 1 \times 10^{11}$ cm^{-2}
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS					
3-4.1	Stacking Faults	≤ 1 cm^{-2}	≤ 0.1 cm^{-2}		≤ 0.03 cm^{-2}
3-4.2,3	Slip/Dislocations	None		Total length ≤diameter/2	None
3-4.4	Large LLS, Size ≥20 µm LSE				

Previous SEMI Reference:		*SEMI M11, Table 3*	*SEMI M11, Table 4*	*SEMI M11, Table 5*	*SEMI M11, Tables 6 and 8*
Design Rule:		*1.0 µm*	*0.35 µm*	*0.35 µm*	*0.25 µm*
Epitaxial Wafer Category:		*11.3*	*11.4*	*11.5*	*11.6*
Technology		*Twin-Tub CMOS*	*Twin-Tub CMOS*	*DRAM*	*Twin-Tub CMOS*
3-4.5	Localized Light Scatterers (LLS)#6,#7	≤0.2 cm^{-2} at ≤0.5 µm LSE	≤0.2 cm^{-2} at ≤0.2 µm LSE	≤0.2 cm^{-2} at ≤0.16 µm LSE	≤0.36 cm^{-2} at ≤0.16 µm LSE
3-4.6	Haze	None			None
3-4.7,8	Scratches – Macro and Micro	None			None
3-4.9	Edge Chips and Indents	None			
3-4.10	Foreign Matter	None			None
3-4.11	Dimples	None			None
3-4.12	Orange Peel	None			None
3-4.16	Cracks, Crow's Feet	None			None
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS					
3-5.1	Contamination	None			

#1 If a choice is listed, selection must be made.

#2 Oxygen concentration per in-process monitoring only.

#3 Backseal may be none or polysilicon, silicon dioxide, or silicon nitride (or a combination, as required) with thickness as specified by customer. For category 11.5 epitaxial wafers, only none or silicon dioxide is permitted. For category 11.6 epitaxial wafers, the choices are as follows: silicon oxide: 5000 ± 1000 Å, polysilicon: 10,000 ± 2000 Å, back surface damage, none, combination of 3000 ± 1000 Å silicon oxide on top of 8000 ± 2000 Å polysilicon.

#4 These properties are not included in Part 2 of the Silicon Wafer Specification Format for Order Entry.

#5 Measurement by mercury probe (SEMI MF1392 or DIN 50439).

#6 Based on calibration of SSIS with PSL spheres (SEMI M53), 90% capture rate.

#7 The requirement for epitaxial wafers of category 11.6 is mathematically consistent with the SIA Roadmap value of 0.6 per cm^2 maximum for LLSs ≥0.12 µm LSE. The SIA Roadmap value was transformed using draft international standard ISO/DIS 14644-1 which follows the equation: 0.36 per cm^2 = 0.60 per cm^2/(0.16 µm /0.125 µm)$^{2.08}$.

Table R2-3 Guide for the Specification of 0.18 µm Design Rule Epitaxial Wafers

Previous SEMI Reference:		*SEMI M11, Table 7*		
Wafer Category:		*11.7.1*	*11.7.2*	*11.7.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.3	Crystal Orientation	(100) ±1°		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.8	Wafer Surface Orientation	Off-orientation 0.6° ± 0.4°		
2-1.6	Nominal Edge Exclusion	3 mm		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm#1	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation	≤20%		
2-3.1	Oxygen Concentration	As agreed between supplier and customer		
	Within shipment variation, Old ASTM	±1.5 ppma	±2.0 ppma#2	
2-3.2	Radial Oxygen Variation	≤10%		

Previous SEMI Reference:		*SEMI M11, Table 7*		
Wafer Category:		*11.7.1*	*11.7.2*	*11.7.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2-3.3	Carbon Concentration	≤0.5 ppma	Not specified[#2]	
2-4.7	Oxidation Induced Stacking Faults	As agreed between supplier and customer		
2-5.1	Wafer ID Marking[#3]	Per substrate category 1.9.1, 1.9.2, or 1.15		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	None	As agreed between supplier and customer	
2-5.7	Edge Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#3]	Per substrate category 1.9.1, 1.9.2, or 1.15 except as noted below:		
2-6.8	Total Thickness Variation (GBIR)	≤3 µm		
2-6.9	Bow	Not specified		
2-6.10	Warp[#4]	≤50 µm for wafers without backseal, ≤100 µm for wafers with backseal		
2-9.8	Back Surface Brightness (Gloss)[#5]	≥80% (for wafers without backseal only)		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	*p/p⁻*	*p/p⁺*	*p/p⁺⁺*
3-1.2	Layer Dopant	Boron		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation	±5% per Equation 4	±10% for wafers without backseal, ±5% for wafers with backseal, both per Equation 4	
3-1.7	Layer Thickness, center point	Target: As agreed between supplier and customer; Tolerance ±5%		
3-1.8	Thickness Variation within wafer	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.6	Flatness, Site	≤0.18 µm, SFSR, 25 mm × 32 mm sites, Include partial sites, No offset		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.1	Stacking Faults	<2 per wafer		
3-4.2,3	Slip/Dislocations[#6]	None		
3-4.5	Localized Light Scatterers (LLS)[#7]	≤60 per wafer at ≥0.09 µm PSL or ≤33per wafer at ≥0.12 µm PSL (300 mm); ≤26 per wafer at ≥0.09 µm PSL or ≤14 per wafer at ≥0.12 µm PSL (200 mm)		
3-4.6	Haze	None		
3-4.7	Scratches — Macro	None		

Previous SEMI Reference:		*SEMI M11, Table 7*		
Wafer Category:		*11.7.1*	*11.7.2*	*11.7.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-4.8	Scratches — Micro	≤10 mm total length		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.16	Cracks, Crow's Feet	None		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	≤25 mm total length		
3-5.4	Localized Light Scatterers (LLS)[#8]	Not specified		
3-5.5	Edge Chips	None		

#1 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#2 Practical nondestructive metrology did not exist at the time this document was approved.

#3 If a choice is listed, selection must be made.

#4 Only process control data required.

#5 Double-side polish preferred on both 200 mm and 300 mm wafers.

#6 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726.

#7 These values are mathematically consistent. The 0.09 µm count limit was transformed using ISO 14644-1, which follows the equation: 34 counts per wafer = 60 counts per wafer / (0.12 µm/0.09 µm)$^{2.08}$. These counts are approximately equivalent to 0.09 counts/cm^2 at 0.09 µm LSE and 0.05 counts/cm^2 at 0.12 µm LSE.

#8 Process control capability is expected to be: ≤500 at ≥0.25 µm LSE.

Table R2-4 Guide for the Specification of 130 nm Design Rule Epitaxial Wafers

Previous SEMI Reference:		*SEMI M11, Table 9*		
Wafer Category:		*11.9.1*	*11.9.2*	*11.9.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.3	Crystal Orientation	(100) ± 1°		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.8	Wafer Surface Orientation	Off-orientation 0.6° ± 0.4°		
2-1.6	Nominal Edge Exclusion	3 mm		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#1]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation	≤20%		
2-3.1	Oxygen Concentration	As agreed between supplier and customer		
	Tolerance, Old ASTM	±2.0 ppma	±2.0 ppma[#2]	
2-3.2	Radial Oxygen Variation	≤10%		
2-3.3	Carbon Concentration	≤0.5 ppma	≤0.5 ppma[#2]	
2-4.7	Oxidation Induced Stacking Faults	Not specified		
2-4.8	Oxide Precipitates, BMD	As agreed between supplier and customer		

Previous SEMI Reference:		*SEMI M11, Table 9*		
Wafer Category:		*11.9.1*	*11.9.2*	*11.9.3*
Technology		*p/p^- (for DRAM)*	*p/p^+ (for DRAM, Logic)*	*p/p^{++} (for Logic)*
2-4.9	Intersititial Oxygen Reduction ($\Delta[O_i]$)	As agreed between supplier and customer		
2-5.1	Wafer ID Marking[#3]	Per substrate category 1.9.1, 1.9.2, or 1.15		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	None	As agreed between supplier and customer	
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#3]	Per substrate category 1.9.1, 1.9.2, or 1.15 except as noted below:		
2-6.9	Bow	Not specified		
2-6.10	Warp[#4]	≤50 µm for wafers without backseal, ≤100 µm for wafers with backseal		
2-9.8	Back Surface Brightness (Gloss)[#5]	≥80% (for wafers without backseal only)		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	p/p^-	p/p^+	p/p^{++}
3-1.2	Layer Dopant	Boron		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: As agreed between supplier and customer; Tolerance ±5%		
3-1.8	Layer Thickness Variation	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.6	Flatness, Site	≤0.13 µm, SFSR, 25 mm × 32 mm sites, Include partial sites, No offset		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{11}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1.3 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.1	Stacking Faults	<0.12 cm^{-2}		
3-4.2,3	Slip/Dislocations[#6]	None		
3-4.4	Large Localized Light Scatterers	<0.006 cm^{-2} (at least one side >1 µm)		
3-4.5	Localized Light Scatterers (LLS)[#7]	≤200 per wafer at ≥0.09 µm PSL or ≤112 per wafer at ≥0.12 µm PSL (300 mm); ≤87 per wafer at ≥0.09 µm PSL or ≤48 per wafer at ≥0.12 µm PSL (200 mm)		
3-4.6	Haze	None		
3-4.7	Scratches — Macro	None		
3-4.8	Scratches — Micro	≤10 mm total length		

Previous SEMI Reference:		*SEMI M11, Table 9*		
Wafer Category:		*11.9.1*	*11.9.2*	*11.9.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.16	Cracks, Crow's Feet	None		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)[#8]	Not specified		
3-5.5	Edge Chips	None		

#1 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#2 Practical non-destructive metrology did not exist at the time this document was approved.

#3 If a choice is listed, selection must be made.

#4 Only process control data required.

#5 Double-side polish preferred on both 200 mm and 300 mm wafers.

#6 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726.

#7 These values are mathematically consistent. The 0.09 µm count limit was transformed using ISO 14644-1, which follows the equation: 34 counts per wafer = 60 counts per wafer / (0.12 µm/0.09 µm)$^{2.08}$. These counts are approximately equivalent to 0.09 counts/cm^2 at 0.09 µm LSE and 0.05 counts/cm^2 at 0.12 µm LSE.

#8 Process control capability is expected to be: ≤500 @ ≥0.25 µm LSE.

Table R2-5 Guide for the Specification of 90 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:		*SEMI M11, Table 10*		
Epitaxial Wafer Category:		*11.10.1*	*11.10.2*	*11.10.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.3	Crystal Orientation	(100) ± 1°		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.8	Wafer Surface Orientation	Off-orientation 0.6° ± 0.4°		
2-1.6	Nominal Edge Exclusion[#1]	3 mm (200 mm wafers), 2 mm (300 mm wafers)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation[#3]	≤20%		
2-3.1	Oxygen Concentration, Center[#4] Tolerance, Old ASTM	As agreed between supplier and customer As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-4.1	Dislocation Etch Pit Density	As agreed between supplier and customer		
2-4.2	Slip	As agreed between supplier and customer		

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Previous SEMI Reference:		*SEMI M11, Table 10*		
Epitaxial Wafer Category:		*11.10.1*	*11.10.2*	*11.10.3*
Technology		*p/p^- (for DRAM)*	*p/p^+ (for DRAM, Logic)*	*p/p^{++} (for Logic)*
2-4.3	Lineage	As agreed between supplier and customer		
2-4.4	Twin Boundary	As agreed between supplier and customer		
2-4.5	Swirl	As agreed between supplier and customer		
2-4.6	Shallow Pits	As agreed between supplier and customer		
2-4.7	Oxidation Induced Stacking Faults	As agreed between supplier and customer		
2-4.8	Oxide Precipitates, BMD	As agreed between supplier and customer		
2-4.9	Intersititial Oxygen Reduction ($\Delta[O_i]$)	As agreed between supplier and customer		
2-5.1	Wafer ID Marking[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm) except as noted below:		
2-6.8	Total Thickness Variation, GBIR	≤3 µm		
2-6.9	Bow	Not specified		
2-6.10	Warp[#3]	≤50 µm for wafers without backseal, ≤100 µm for wafers with backseal		
2-9.8	Back Surface Brightness (Gloss)[#7]	≥80% (for wafers without backseal only)		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	p/p^-	p/p^+	p/p^{++}
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: As agreed between supplier and customer; Tolerance: ±5%		
3-1.8	Layer Thickness Variation	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#8]	≤50 µm		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤4 µm		
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR[#6]	≤90 nm, 26 mm × 8 mm sites, ≥95% usable area, partial sites included, no offset OR 100% usable area, full sites only, no offset		
3-2.7	Nanotopography	As agreed between supplier and customer for both 2 mm and 10 mm diameter analysis areas		
3-2.8	Misfit Dislocations	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		

Previous SEMI Reference:		*SEMI M11, Table 10*		
Epitaxial Wafer Category:		*11.10.1*	*11.10.2*	*11.10.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#9]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS), count per wafer[#10]	≤238 at ≥90 nm PSL; ≤10 at ≥300 nm PSL; ≤5 at ≥2 µm (300 mm); ≤102 at ≥90 nm PSL; ≤4 at ≥300 nm PSL, ≤2 at 2 µm PSL (200 mm)		
3-4.6	Haze	None		
3-4.7	Scratches – Macro	None		
3-4.8	Scratches – Micro	None		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		
3-4.20	Stains	None		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.6	Cracks, Crow's Feet	None		
3-5.7	Saw Marks	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by

SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 This specification implies a polished back surface.

#8 Only process control data is required. Data not required on Certificate of Compliance. A larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#9 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at less ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in 90 nm technology thermal processes, slip propagation should not be a problem.

#10 The 90 nm count, 238, is from the 2003 ITRS 90 nm node. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at x nm = (count per wafer at y nm) × (y nm/x nm)$^{2.08}$. For example converting from a 90 nm minimum size to a 65 nm minimum size yields a new count of 456. The counts for 90 nm and 200 nm LSE sizes may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

Table R2-6 Guide for the Specification of 65 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.11.1*	*11.11.2*	*11.11.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.2	Use of Refined Polysilicon	Permitted		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.6	Nominal Edge Exclusion[#1]	3 mm (200 mm wafers), 2 mm (300 mm wafers)		
2-1.8	Wafer Surface Orientation	{100} off orientation (0.6° ± 0.4°)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation[#3]	≤20%		
2-3.1	Oxygen Concentration, Center[#4] Tolerance	As agreed between supplier and customer As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-5.1	Wafer ID Marking[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-5.8	Back Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm) except as noted below:		
2-6.1	Diameter	300 ± 0.20 mm or 200 ± 0.20 mm		
2-6.2	Fiducial Dimensions	In accordance with requirement of wafer category 1.15 (see SEMI M1, figure 5)		
2-6.3	Primary Flat/Notch Orientation	<110> ± 1º		
2-6.7	Thickness	775 ± 20 µm (300 mm) or 725 ± 20 µm (200 mm)		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.11.1*	*11.11.2*	*11.11.3*
Technology		*p/p^- (for DRAM)*	*p/p^+ (for DRAM, Logic)*	*p/p^{++} (for Logic)*
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	p/p^-	p/p^+	p/p^{++}
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: As agreed between supplier and customer; Tolerance: ±5%		
3-1.8	Layer Thickness Variation	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#7]	≤50 µm		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤4 µm		
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR[#6]	≤65 nm, 26 mm × 8 mm sites, ≥95% usable area, partial sites included, no offset OR 100% usable area, full sites only, no offset		
3-2.7	Nanotopography	As agreed between supplier and customer for both 2 mm and 10 mm diameter analysis areas		
3-2.9	Flatness, Site, SBIR	As agreed between supplier and customer		
3-2.10	Edge Profile	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#8]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS), count per wafer[#9]	≤123 at ≥90 nm PSL; ≤10 at ≥300 nm PSL ≤53 at ≥90 nm PSL; ≤4 at ≥300 nm PSL		
3-4.6	Haze	None		
3-4.7	Scratches — Macro	None		
3-4.8	Scratches — Micro	As agreed between supplier and customer		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.11.1*	*11.11.2*	*11.11.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		
3-4.20	Stains	None		
3-4.21	Misfits	As agreed between supplier and customer		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches — Macro	None		
3-5.3	Scratches — Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.6	Cracks, Crow's Feet	None		
3-5.7	Saw Marks	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 A larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#8 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at less ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in 90 nm technology thermal processes, slip propagation should not be a problem.

#9 The 90 nm count, 123, is from the 2005 ITRS 65 nm node. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at x nm = (count per wafer at y nm) × (y nm/x nm)$^{2.08}$. The counts for 90 nm and 300 nm LSE sizes may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

Table R2-7 Guide for the Specification of 45 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:	*None*		
Epitaxial Wafer Category:	*11.12.1*	*11.12.2*	*11.12.3*
Technology	*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS			

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134-2127
Phone: 408.943.6900, Fax: 408.943.7943

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Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.12.1*	*11.12.2*	*11.12.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.2	Use of Refined Polysilicon	Permitted		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.6	Nominal Edge Exclusion[#1]	3 mm (200 mm wafers), 2 mm (300 mm wafers)		
2-1.8	Wafer Surface Orientation	{100} off orientation (0.6° ± 0.4°)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation[#3]	≤20%		
2-3.1	Oxygen Concentration, Center[#4]	As agreed between supplier and customer		
	Tolerance	As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-5.1	Wafer ID Marking[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-5.8	Back Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per substrate category 1.9.1 or 1.9.2 (200 mm), or 1.15 (300 mm) except as noted below:		
2-6.1	Diameter	300 ± 0.20 mm or 200 ± 0.20 mm		
2-6.2	Fiducial Dimensions	In accordance with requirement of wafer category 1.15 (see SEMI M1 Figure 5)		
2-6.3	Primary Flat/Notch Orientation	<110> ± 1°		
2-6.7	Thickness	775 ± 20 µm (300 mm) or 725 ± 20 µm (200 mm)		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	*p/p⁻*	*p/p⁺*	*p/p⁺⁺*
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: As agreed between supplier and customer; Tolerance: ±5%		
3-1.8	Layer Thickness Variation	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#7]	≤50 µm		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤4 µm		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.12.1*	*11.12.2*	*11.12.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR[#6]	≤45 nm, 26 mm × 8 mm sites, ≥95% usable area, partial sites included, no offset, OR 100% usable area, full sites only, no offset		
3-2.7	Nanotopography	As agreed between supplier and customer for both 2 mm and 10 mm diameter analysis areas		
3-2.9	Flatness, Site, SBIR	As agreed between supplier and customer		
3-2.10	Edge Profile	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#8]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS), count per wafer[#9]	≤115 at ≥65 nm PSL; ≤10 at ≥ For Area Defects (Area defect definition to be agreed upon between supplier and customer) ≤49 at ≥65 nm PSL, ≤4 at For Area Defects (Area defect definition to be agreed upon between supplier and customer)		
3-4.6	Haze	None		
3-4.7	Scratches — Macro	None		
3-4.8	Scratches — Micro	As agreed between supplier and customer		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		
3-4.20	Stains	None		
3-4.21	Misfits	As agreed between supplier and customer		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.12.1*	*11.12.2*	*11.12.3*
Technology		*p/p⁻ (for DRAM)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.6	Cracks, Crow's Feet	None		
3-5.7	Saw Marks	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 Only process control data is required. Data not required on Certificate of Compliance. A larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#8 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at less ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in 90 nm technology thermal processes, slip propagation should not be a problem.

#9 The 65 nm count, 115, is from the 2005 ITRS 45 nm node. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at x nm = (count per wafer at y nm) × (y nm/x nm)$^{2.08}$. The counts for 65 nm and Area Defect size may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

Table R2-8 Guide for the Specification of 32 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.13.1*	*11.13.2*	*11.13.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.2	Use of Refined Polysilicon	Permitted		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.6	Nominal Edge Exclusion[#1]	2 mm (300 mm wafers)		
2-1.8	Wafer Surface Orientation	{100} off orientation (0.6° ± 0.4°)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation[#3]	≤20%		
2-3.1	Oxygen Concentration, Center[#4]	As agreed between supplier and customer		
	Tolerance	As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.13.1*	*11.13.2*	*11.13.3*
Technology		*p/p^- (for DRAM Logic)*	*p/p^+ (for DRAM, Logic)*	*p/p^{++} (for Logic)*
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-5.1	Wafer ID Marking[#6]	Per (SEMI M1) substrate category 1.15 (300 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-5.8	Back Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per (SEMI M1) substrate category 1.15 (300 mm)		
2-6.1	Diameter	300 ± 0.2 mm		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	p/p^-	p/p^+	p/p^{++}
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation[#7]	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: Customer Specified; Tolerance: ±5%		
3-1.8	Layer Thickness Variation	±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#8]	≤50 µm for wafers without backseal		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤4 µm		
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR[#6]	≤32 nm, 26 mm × 8 mm sites, ≥95% usable area by shipment sample, partial sites included, no offset, OR 100% usable area, full sites only, no offset		
3-2.7	Nanotopography[#9]	≤8 nm (2 mm × 2 mm)		
3-2.9	Flatness, Site, SBIR	As agreed between supplier and customer		
3-2.10	Edge Profile	As agreed between supplier and customer		
3-2.11	Edge Roll-off	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.13.1*	*11.13.2*	*11.13.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#9]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS), count per wafer[#11]	≤110 at ≥45 nm PSL; ≤10 at ≥150 nm PSL (300 mm)		
3-4.6	Haze	None		
3-4.7	Scratches — Macro	None		
3-4.8	Scratches — Micro	As agreed between supplier and customer		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		
3-4.20	Stains	None		
3-4.21	Misfits	As agreed between supplier and customer		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.6	Cracks, Crow's Feet	None		
3-5.7	Saw Marks	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 Subject to measurement capability near the edge.

#8 Larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#9 Measurement Method SEMI M78. The nanotopography values generally follow ITRS using node values for DRAM ½ pitch. These values are considered challenging. If desired, different nanotopography specifications may be agreed upon between supplier and customer.

#10 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in ≤90 nm technology thermal processes, slip propagation should not be a problem.

#11 ITRS 2009 recommends a count of 110 for 32 nm node. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at x nm = (count per wafer at y nm) × (y nm/x nm)$^{2.08}$. The counts for 32 nm and 150 nm LSE sizes may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

Table R2-9 Guide for the Specification of 22 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.14.1*	*11.14.2*	*11.14.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.2	Use of Refined Polysilicon	Permitted		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.6	Nominal Edge Exclusion[#1]	2 mm (300 and 450 mm wafers)		
2-1.8	Wafer Surface Orientation	{100} off orientation (0.6° ± 0.4°)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2-2.2	Radial Resistivity Variation[#3]	≤10%		
2-3.1	Oxygen Concentration, Center[#4]	As agreed between supplier and customer		
	Tolerance	As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-5.1	Wafer ID Marking[#6]	Per (SEMI M1) substrate category 1.15 (300 mm); SEMI T7 (450 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-5.8	Back Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per (SEMI M1) substrate category 1.15 (300 mm) and 1.16.1 (450 mm)		
2-6.1	Diameter	300 ± 0.20 mm or 450 ± 0.10 mm		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	*p/p⁻*	*p/p⁺*	*p/p⁺⁺*
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation[#7]	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: Customer Specified; Tolerance: < ±5%		
3-1.8	Layer Thickness Variation	< ±10% per Equation 2		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.14.1*	*11.14.2*	*11.14.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#8]	≤50 µm for wafers without backseal		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤3 µm		
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR	≤22 nm, 26 mm × 8 mm sites, PUA and partial sites inclusion As agreed between supplier and customer		
3-2.7	Nanotopography[#9]	≤6 nm (2 mm × 2 mm)		
3-2.9	Flatness, Site, SBIR	As agreed between supplier and customer		
3-2.10	Edge Profile	As agreed between supplier and customer		
3-2.11	Edge Roll-off	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#10]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS)[#11]	≤0.19 cm^{-2} @ ≥32 nm LSE (Measurement sensitivity and dependence on epi surface condition may need to be verified)		
3-4.6	Haze	None		
3-4.7	Scratches – Macro	None		
3-4.8	Scratches – Micro	As agreed between supplier and customer		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.14.1*	*11.14.2*	*11.14.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-4.20	Stains	None		
3-4.21	Misfits	As agreed between supplier and customer		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 Subject to measurement capability near the edge.

#8 Larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#9 considered challenging. If desired, different nanotopography specifications may be agreed upon between supplier and customer.

#10 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in ≤90 nm technology thermal processes, slip propagation should not be a problem.

#11 ITRS 2009 recommends a count of 126 for 22 nm node at ≥22 nm sensitivity. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at x nm = (count per wafer at y nm) × (y nm/x nm)$^{2.08}$. The counts for 22 nm and 150 nm Latex Sphere Equivalent (LSE) sizes may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

Table R2-10 Guide for the Specification of 16 nm Design Rule Epitaxial Wafers with DSP Substrates

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.15.1*	*11.15.2*	*11.15.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
2. SUBSTRATE CHARACTERISTICS				
2-1.1	Growth Method	Supplier option of Cz or MCz		
2-1.2	Use of Refined Polysilicon	Permitted		
2-1.4	Conductivity Type	*p*		
2-1.5	Dopant	Boron		
2-1.6	Nominal Edge Exclusion[#1]	2 mm (300 and 450 mm wafers)		
2-1.8	Wafer Surface Orientation	{100} off orientation (0.6° ± 0.4°)		
2-2.1	Resistivity, Center point	0.8–15 Ω·cm[#2]	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.15.1*	*11.15.2*	*11.15.3*
Technology		*p/p^- (for DRAM Logic)*	*p/p^+ (for DRAM, Logic)*	*p/p^{++} (for Logic)*
2-2.2	Radial Resistivity Variation[#3]	≤10%		
2-3.1	Oxygen Concentration, Center[#4]	As agreed between supplier and customer		
	Tolerance	As agreed between supplier and customer		
2-3.2	Radial Oxygen Variation[#5]	As agreed between supplier and customer		
2-3.3	Carbon Concentration, Background[#3, #4]	≤0.5 ppma		
2-5.1	Wafer ID Marking[#6]	Per (SEMI M1) substrate category 1.15 (300 mm); SEMI T7 (450 mm)		
2-5.3	Denuded Zone	As agreed between supplier and customer		
2-5.4	Extrinsic Gettering	As agreed between supplier and customer		
2-5.5	Backseal	As agreed between supplier and customer		
2-5.6	Annealing	As agreed between supplier and customer		
2-5.7	Edge Surface Condition	Polished		
2-5.8	Back Surface Condition	Polished		
2-6.	Wafer Dimensional Characteristics[#6]	Per (SEMI M1) substrate category 1.15.1 (300 mm) and 1.16.1 (450 mm)		
2-6.1	Diameter	300 ± 0.20mm or 450 ± 0.10mm		
3-1. GENERAL EPTIAXIAL WAFER AND LAYER CHARACTERISTICS				
3-1.1	Conductivity Type/Structure	p/p^-	p/p^+	p/p^{++}
3-1.2	Layer Dopant	Boron		
3-1.3	Silicon Source Gas	As agreed between supplier and customer		
3-1.4	Layer Growth Method	As agreed between supplier and customer		
3-1.5	Layer Net Carrier Density Range	As agreed between supplier and customer		
3-1.6	Net Carrier Density Variation[#7]	Net carrier density must be within range at all points in the FQA		
3-1.7	Layer Thickness, center point	Target: Customer Specified; Tolerance: < ±5%		
3-1.8	Layer Thickness Variation	< ±10% per Equation 2		
3-1.9	Transition Width	As agreed between supplier and customer		
3-1.10	Flat Zone	As agreed between supplier and customer		
3-2. POST-EPI DIMENSIONAL CHARACTERISTICS				
3-2.1	Bow	As agreed between supplier and customer		
3-2.2	Warp[#8]	≤50 µm for wafers without back seal		
3-2.3	Sori	As agreed between supplier and customer		
3-2.4	Total Thickness Variation, GBIR	≤3 µm		
3-2.5	Flatness, Global, GFLR	≤3 µm		
3-2.6	Flatness, Site, SFQR	≤20 nm, 26 mm × 8 mm sites, PUA and partial sites inclusion as agreed between supplier and customer		
3-2.7	Nanotopography[#9]	≤5 nm (2 mm × 2 mm)		
3-2.9	Flatness, Site, SBIR	As agreed between supplier and customer		
3-2.10	Edge Profile	As agreed between supplier and customer		
3-2.11	Edge Roll-off	As agreed between supplier and customer		
3-3. POST-EPI FRONT SURFACE CHEMISTRY				
3-3.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.3	Potassium	$\leq 1 \times 10^{10}$ cm^{-2}		

Previous SEMI Reference:		*None*		
Epitaxial Wafer Category:		*11.15.1*	*11.15.2*	*11.15.3*
Technology		*p/p⁻ (for DRAM Logic)*	*p/p⁺ (for DRAM, Logic)*	*p/p⁺⁺ (for Logic)*
3-3.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.8	Zinc	$\leq 1 \times 10^{10}$ cm^{-2}		
3-3.1.9	Calcium	$\leq 1 \times 10^{10}$ cm^{-2}		
3-4. POST-EPI FRONT SURFACE INSPECTION CHARACTERISTICS				
3-4.2	Slip[#10]	None		
3-4.3	Dislocations	None		
3-4.5	Localized Light Scatterers (LLS)[#11]	≤ 0.18 cm^{-2} @ ≥ 32 nm LSE (Measurement sensitivity and dependence on epi surface condition may need to be verified)		
3-4.6	Haze	None		
3-4.7	Scratches – Macro	None		
3-4.8	Scratches – Micro	As agreed between supplier and customer		
3-4.9	Edge Chips and Indents	None		
3-4.10	Foreign Matter	None		
3-4.11	Dimples	None		
3-4.12	Orange Peel	None		
3-4.13	Contamination/Area	None		
3-4.14	Edge Cracks	None		
3-4.15	Edge Crown	None		
3-4.16	Cracks, Crow's Feet	None		
3-4.18	Saw Marks	None		
3-4.19	Dopant Striation Rings	None		
3-4.20	Stains	None		
3-4.21	Misfits	As agreed between supplier and customer		
3-5. POST-EPI BACK SURFACE INSPECTION CHARACTERISTICS				
3-5.1	Contamination	None		
3-5.2	Scratches – Macro	None		
3-5.3	Scratches – Micro	Cumulative length ≤10% of wafer diameter		
3-5.4	Localized Light Scatterers (LLS)	Not specified		
3-5.5	Edge Chips	None		
3-5.8	Stains	None		

#1 Unless otherwise agreed upon for a specific characteristic or test method.

#2 Resistivity of substrate shall be chosen to match resistivity of epitaxial layer.

#3 Only process control data is required. Data not required on Certificate of Compliance.

#4 Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates. Measurements of oxygen level on lightly doped substrates should be made by SEMI MF1188, JEIDA 61, or DIN 50438-1. Measurements of oxygen level on heavily doped substrates should be made by SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and customer. Practical nondestructive metrology for oxygen measurements on heavily doped substrates did not exist at the time this document was approved.

#5 Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

#6 If a choice is listed, selection must be made.

#7 Subject to measurement capability near the edge.

#8 Larger warp value may be appropriate if an oxide layer is deposited on the back of the substrate.

#9 Measurement Method SEMI M78. The nanotopography values generally follow ITRS using node values for DRAM ½ pitch. These values are considered challenging. If desired, different nanotopography specifications may be agreed upon between supplier and customer.

#10 An etch depth <100 nm is acceptable when testing in accordance with SEMI MF1726. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the etching and microscopic inspection method given in SEMI MF1726, but no standard test method currently exists. X-ray topography can detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at ≤90 nm can also reveal slip lines on epitaxial wafers but again no standard test method currently exists. Surface roughness may interfere with SSIS measurements. However, with the thermal cycles employed in ≤90 nm technology thermal processes, slip propagation should not be a problem.

#11 ITRS 2009 recommends a count of 127 (300 mm wafer) and 286 (450 mm wafer) for 16nm node at ≥ 32nm sensitivity. This count may be transformed to a count at another size using ISO 14644-1, which uses the equation: count per wafer at *x* nm = (count per wafer at *y* nm) × (*y* nm/*x* nm)$^{2.08}$. The counts for 32 nm and 150 nm Latex Sphere Equivalent (LSE) sizes may include stacking faults of different scattering intensities and other structural epitaxial defects that are not correctly sized by current generation SSISs.

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