Background Statement for SEMI Draft Document 5727

New Standard: Test Method for the Etch Rate of A Crystalline Silicon Wafer by Determining the Weight Loss

Notice: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this Document.

Notice: Recipients of this Document are invited to submit, with their comments, notification of any relevant patented technology or copyrighted items of which they are aware and to provide supporting documentation. In this context, “patented technology” is defined as technology for which a patent has issued or has been applied for. In the latter case, only publicly available information on the contents of the patent application is to be provided.

Background statement:
Test method of etch rate, getting mass difference through weight method, using the density and volume formulas, calculating the etch rate.
The test method of solar cell's etching rate has been used in solar cell production including etch, edge isolation etch, silicon wafer’s polishing process etc. at present.
Whether produce or research of high efficiency cells, test method for etch rate of silicon wafer will be used, But there are no the relevant international standards, result in no files are accorded during production or research, the test method of silicon wafer etch rate by determining the weight loss has been used in the industry widely. But there are no unified standard, the standard is needed completion urgently to get the stability of production quality goal.

Review and Adjudication Information

<table>
<thead>
<tr>
<th>Task Force Review</th>
<th>Committee Adjudication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group:</td>
<td>Crystalline Silicon Solar Cell Task Force</td>
</tr>
<tr>
<td>Date:</td>
<td>February 20th, 2015</td>
</tr>
<tr>
<td>Time &amp; Time zone:</td>
<td>9:00—11:30</td>
</tr>
<tr>
<td>Location:</td>
<td>Telephone Conference</td>
</tr>
<tr>
<td>City, State/Country:</td>
<td>China</td>
</tr>
<tr>
<td>Leader(s):</td>
<td>Song Dengyuan (Yingli)</td>
</tr>
<tr>
<td></td>
<td>Chen Rulong (Suntech)</td>
</tr>
<tr>
<td></td>
<td>Cai Xianwu (CETC48)</td>
</tr>
<tr>
<td>Standards Staff:</td>
<td>Kris Shen(SEMI China)</td>
</tr>
<tr>
<td></td>
<td><a href="mailto:kshen@semi.org">kshen@semi.org</a></td>
</tr>
</tbody>
</table>

Meeting date and time are subject to change, and additional TF review sessions may be scheduled if necessary. Contact the task force leaders or Standards staff for confirmation.
Check [www.semi.org/standards](http://www.semi.org/standards) for the latest schedule.

If you have any questions, please contact the ballot author at:
Fengxia Sun/ Yingli
Tel: +86 139 3324 7890
E-mail: fx.sun@yingli.com

Yingye Li/ Yingli
Tel: +86 137 2223 9055
E-mail: yingye.li@yingli.com
SEMI Draft Document 5727
New Standard: Test Method for the Etch Rate of a Crystalline Silicon Wafer by Determining the Weight Loss

1 Purpose

1.1 The purpose of this standard is to standardize a fast and accurate test method for the etch rate of a crystalline silicon wafer by determining the weight loss.

2 Scope

2.1 This standard specifies the test method of crystalline silicon wafer etch, edge isolation etch, polishing and other corrosion rate.

2.2 This standard applies to the testing of etch rate in the process of making cells.

2.3 This standard specifies the corrosion time.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 ISO Standard

ISO 14644-1—1999 — Cleanrooms and Associated Controlled Environments — Part 1: Classification of Air Cleanliness.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions

4.1.1 Crystalline Silicon Wafer Etch — the phenomena that silicon surface material is destroyed, due to chemical reaction with around liquid in the wafer cleaning step.

4.1.2 Edge Isolation Etch — achieve insulation of both sides of after the semi-finished solar cell with chemical methods.

4.1.3 Etch Rate — what loss of weight per unit area of materials in unit time.

4.1.4 Depth of Etch — the average depth of the sample surface damage layer.

5 Summary of Test Method

Choose the appropriate acid solution contact with silicon material samples for chemical etch, record etch times, and mass difference before and after etch with electronic balance, etch depth of the sample is obtained by formula (1), Formula (3) is deduced by the formula (2), calculate the etch rate through the formula (3).

5.1 The etch rate is derived through corrosion depth:

$$\Delta h = \frac{W_1 - W_2}{S \times \rho}$$  \hspace{1cm} (1)

Where:

$\Delta h$ — Corrosion depth after the etch of wafer, \( \mu \text{m} \);

$W_1$ — Original weight of sample, g;

$W_2$ — Weight of the sample after removal of surface corrosion, g;

---

1 International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch
\[ \rho \text{ — Density of silicon, g/cm}^3; \]
\[ S \text{ — Double-sided Corrosion area of the sample, cm}^2; \]
\[ \Delta h = v \times T \]

Where:

\[ v \text{ — Etch rate, \( \mu m/s \);} \]
\[ T \text{ — Time of etched, s;} \]
\[ \Delta h \text{ — Corrosion depth after the etch of wafer, \( \mu m \);} \]

\[ v = \frac{W_1 - W_2}{S \times T \times \rho} \]

Where:

\[ v \text{ — Etch rate, \( \mu m/s \);} \]
\[ W_1 \text{ — Original weight of sample, g;} \]
\[ W_2 \text{ — Weight of the sample after removal of surface corrosion, g;} \]
\[ S \text{ — Double-sided Corrosion area of the sample, cm}^2; \]
\[ T \text{ — Time of etched, s;} \]
\[ \rho \text{ — Density of silicon, g/cm}^3. \]

6 Apparatus

6.1 *Electronic Balance* — Range (0-220) grams, Readability 0.0001 g, Repeatability 0.0001 g, Tolerance ± 0.0002 g.

7 Safety Precautions

7.1 Power switch and power outlet of the balance are checked in security before and after use.

8 Test Specimens

8.1 Take same batch wafers to be etched load in carrier cassette, select each piece of one from both end and the middle position, total take 3 pieces. Identify separately.

9 Preparation of Apparatus

9.1 Because of the high sensitivity of the crystalline silicon wafer surface, the testing environment should meet the following requirements:

9.1.1 Environment temperature should be 25°C ± 2°C, and relative humidity 60% ± 20%.

9.1.2 Environmental cleanliness should be better than 4 grade clean room requirements as defined in ISO 14644-1-1999 “Cleanrooms and associated controlled environments — Part 1: Classification of air cleanliness”.

10 Calibration and Standardization

10.1 The balance is zero calibration before using the electronic balance.

11 Procedure

11.1 Choose three wafers from same batch, and put them in different slide box separately.

11.2 Each one clean sample is placed in electronic balance after being calibrated weighing, and record data as \( W_1 \).

11.3 The samples of wafers after being etched and dried are weighed with electronic balance, and record data as \( W_2 \).

11.4 Calculate quality difference before and after etch with formula (4), and record as \( \Delta W \).
\[ \Delta W = W_1 - W_2 \]  

(4)

Where:

\( \Delta W \) — Quality difference before and after etch, g;
\( W_1 \) — Original weight of sample, g;
\( W_2 \) — Weight of the sample after removal of surface corrosion, g.

11.5 Calculate the sample etch depth with formula (1).

11.6 Report etch time during etch.

11.7 The sample etch rate is calculated with formula (2) and (3), and record data.

11.8 The etch rate of rest two samples are tested and recorded continuously with the above steps. Average value of three samples is calculated.

12 Calculations

12.1 The etch rate of sample is calculated according to the formula (5):

\[ v = \frac{V_1 + V_2 + \cdots + V_n}{n} \]  

(5)

Where:

\( v \) — Average value of etch rate, μm/s;
\( V_n \) — Etch rate of 3 test sample, μm/s;
\( n = 3 \).

13 Report

13.1 A title;
13.2 Name and address of the;
13.3 Description and identification of the item tested, including the specimen size;
13.4 Characterization and condition of the test item;
13.5 Date of receipt of test item and date of test, where appropriate;
13.6 Identification of test method used;
13.7 Reference to sampling procedure, where relevant.

NOTICE: Semiconductor Equipment and Materials International (SEMI) makes no warranties or representations as to the suitability of the Standards and Safety Guidelines set forth herein for any particular application. The determination of the suitability of the Standard or Safety Guideline is solely the responsibility of the user. Users are cautioned to refer to manufacturer’s instructions, product labels, product data sheets, and other relevant literature, respecting any materials or equipment mentioned herein. Standards and Safety Guidelines are subject to change without notice.

By publication of this Standard or Safety Guideline, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any items mentioned in this Standard or Safety Guideline. Users of this Standard or Safety Guideline are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights are entirely their own responsibility.