Background Statement for SEMI Draft Document 5474

**Line Item Revision of SEMI 3D6-0913, GUIDE FOR CMP AND MICRO-BUMP PROCESSES FOR FRONTSIDE THROUGH SILICON VIA (TSV) INTEGRATION**

**NOTICE**: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this Document.

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**Background Statement:**

This Line-Item Letter Ballot is issued in accordance with the Special Procedure of Appendix A4, § A4-1 of the *Procedure Manual* to correct nonconforming titles, and concomitant main body text, of published Standards Documents for which it is responsible. It is to be used at the time a Letter Ballot is to be issued for a Standards Documents with a nonconforming title as result of its five-year review or as part of a proposed revision.

According to the SEMI Standards *Procedure Manual*, a Line Item Letter Ballot should include the Purpose, Scope, Limitations, and Terminology sections, along with the full text of any paragraph in which editorial updates are being made.

The 3D P&I TW TC Chapter reviewed and recommended to issue for line item revision ballot.

Review and Adjudication Information

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|  | **Task Force Review** | **Committee Adjudication** |
| **Group:** | Middle End Process Task Force | Taiwan 3DS-IC Committee |
| **Date:** | TBD | Tuesday, September 25, 2018 |
| **Time & Time zone:** | TBD | 14:30-16:00 |
| **Location:** | TBD | SEMI Taiwan Office |
| **City, State/Country:** | Hsinchu/Taiwan | Hsinchu/Taiwan |
| **Leader(s):** | Arthur Chen (NTUST)  Mike Chang (ITRI) | Chien-Chung Lin (ITRI)  Wendy Chen (King Yuan Electronics)  Roger Hwang (ASE) |
| **Standards Staff:** | Dean Chang (SEMI Taiwan)  dchang@semi.org | Dean Chang (SEMI Taiwan)  dchang@semi.org |

This meeting’s details are subject to change, and additional review sessions may be scheduled if necessary. Contact Standards staff for confirmation.

Telephone and web information will be distributed to interested parties as the meeting date approaches. If you will not be able to attend these meetings in person but would like to participate by telephone/web, please contact Standards staff.

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**LINE ITEM 1**: Correct title and concomitant text.

**Notice:** Additions are indicated by underline and deletions are indicated by ~~strikethrough~~

1. **Purpose**
   1. In order to speed up volume production of 3DS-IC products, a generic middle-end process flow is needed to communicate the frontend and backend processes. The quality criteria and metrology methodology of the key modules such as TSV, chemical mechanical planarization (CMP), and micro-bump are developed to ensure high-yield of the middle-end process. Therefore, this guide provides a generic middle-end process flow to define acceptable TSV and CMP quality criteria as well as to develop methodology and measuring procedures for micro-bump. The guide will provide criteria and common baselines of the middle-end process for related upstream and downstream manufacturers in fabricating 3DS-IC products.
2. Scope
   1. This Guide proposes a frontside TSV integration scheme as one of the generic middle-end process flow. The flow includes steps such as TSV formation, RDL formation, CMP, temporary carrier bonding, wafer thinning, micro-bump formation, and carrier debonding.
   2. This Guide define acceptable CMP criteria of TSV in terms of dishing, erosion, and voids. CMP criteria can be determined by metrology technology in both contact methods such as: micro profilometer; 4-points resistivity probes; or non-contact methods (e.g., ultrasonic scan mapping, Coherence Interferometry, or other laser-based light scattering detection schemes). TSV formation and reveal are significantly dependent on the performance of CMP process. The outcome of the high CMP quality yields better TSV connectivity.
   3. This Guide provides criteria for measurement methodology for micro-bump dimensions, including sampling rate, sampling sites and mapping, reference datum, and survey available metrology tools. The outcome will be an important bridge communication among IC design firms, fabs, and packaging houses. The assumption of wafer-to-wafer (W2W), chip-to-wafer (C2W) and chip-to-chip (C2C) are that testing data is available for known test good die.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

1. Limitations
   1. This Guide does not describe dimensions and procedures related to wafers and wafer stacks other than notched, 300 mm nominal diameter.
   2. This Guide does not specify details of the process recipe.
2. Referenced Standards and Documents
   1. *SEMI Standards and Safety Guidelines*

SEMI M59 — Terminology for Silicon Technology

SEMI 3D1 — Terminology for Through Silicon Via Geometrical Metrology

* 1. *JEDEC*[[1]](#footnote-1) *Standards*

JEP158 — 3D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Understanding and Evaluating Reliability Interactions

JESD229 — Wide I/O Single Data Rate (Wide I/O SDR)

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

1. Terminology
   1. Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59 as well as the SEMI Standards Compilation of Terms. Most of these terms and acronyms can be applied to wafers in a 3DS-IC process.
   2. *Abbreviations and Acronyms*
      1. *BUB* — backside micro-bump
      2. *BVR* — backside via reveal
      3. *EDP* — end-point
      4. *FIC* — frontside interconnect contact
      5. *FRDL* — frontside redistribution layer
      6. *FUB* — frontside micro-bump
      7. *MEOL* — middle end of line
      8. *NU* — non-uniformity
      9. *PR* — photo resist
      10. *Ra* — surface roughness
      11. *Rmax* — max surface roughness variation
      12. *RDL* — redistribution layer
      13. *THK* — thickness
      14. *TTV* — total thickness variation
      15. *UB* — micro bump
      16. *WAT* — wafer acceptance test

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1. Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: 703.907.7560, Fax: 703.907.7583, <http://www.jedec.org> [↑](#footnote-ref-1)