SEMI Draft Document 5441
LINE ITEMS REVISION TO SEMI M1-0812
SPECIFICATIONS FOR POLISHED SINGLE CRYSTAL SILICON WAFERS

Notice: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this document.

Notice: Recipients of this document are invited to submit, with their comments, notification of any relevant patented technology or copyrighted items of which they are aware and to provide supporting documentation. In this context, "patented technology" is defined as technology for which a patent has issued or has been applied for. In the latter case, only publicly available information on the contents of the patent application is to be provided.

Background:

This revision is intended with three line items:

(1) to remove reference to the template method of verifying that parameter-based edge profiles are within the specification and to replace the Appendix that describes how to construct the template with a Related Information section that gives a procedure for drawing the edge-shape envelope of wafers with parameter-based edge profiles. This is because the template method is not correct and is not currently being used in the industry, but it was felt that it would be useful to individuals designing equipment to have a better indication of the extent of edge profile variations. This revision, which also includes revision of the material in ¶¶ 6.6 through 6.6.3.4 in order to make it easier to understand and elimination of redundant material related to the edge profile, is being balloted as Line Item 1. **This line item includes all changes in Section 2.6 of Table 1 (including addition of two new footnotes), in ¶¶ 6.6 through 6.6.3.4 including rearrangement of Tables 3 through 11, and in ¶ R4-7.5 as well as removal of Appendix 3 and addition of Related Information 2.**

(2) to remove § 7 (Basic Specification Without Optional Requirements) in its entirety. This 300 mm wafer specification was established for enabling the cost effective production of 300 mm silicon wafer for general use, about seven to eight years ago. Actually, however, this specification is no longer appropriate for manufacturing wafers with optimized device performance. Since it was introduced, several advances in the specification of silicon wafers, including inclusion of edge roll off characteristics and improved edge profile definition, have been made. Therefore this basic specification no longer serves the intended need. This revision is being balloted as Line Item 2. **This line item includes only removal of ¶2.5 and § 7.**

(3) Clean up a number of editorial issues, including the replacement of withdrawn SEMI M6 with SEMI PV22, and other format modifications. This revision is being balloted as Line Item 3. **This line item includes all other changes in the document. (See ¶¶ 2.1, 3.1, R3-3.1, R4-7.6 (Note 1), R4-7.7 (including removal of Note 6), and Footnote 3; §§ A1-1, A2-1, A2-2, A3-1, R3-1, and R4-1.)**

This revision is being balloted in cycle 6 of 2012. Results of this ballot will be reviewed by the International Polished Wafer Task Force and adjudicated by the Japan Silicon Wafer Committee during their meetings at SEMICON® Japan in December 2012. Preliminary results will also be discussed at the NA fall meeting of the International Polished Wafer Task Force at Intel in Santa Clara, CA, on October 29, 2012.

Check www.semi.org/standards for the latest schedule.

For question on the ballot, contact SEMI Staff, Kevin Nguyen at knguyen@semi.org

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DRAFT
Document Number: 5441
Date: 8/28/2012

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SEMI Draft Document 5441
LINE ITEMS REVISION TO SEMI M1-0812
SPECIFICATIONS FOR POLISHED SINGLE CRYSTAL SILICON WAFERS

This Standard was technically approved by the global Silicon Wafer Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on [date tbd]. Available at www.semiviews.org and www.semi.org in [date tbd]; originally published in 1978; previously published August 2012.

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1 Purpose

1.1 Single crystal silicon wafers are utilized for essentially all integrated circuits and many other semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the wafer dimensions to be standardized.

1.2 In addition, as technology advances to smaller and smaller dimensions for the elements of high-density integrated circuits, it has become of interest to standardize additional properties of the wafers.

1.3 This Specification provides the essential dimensional and certain other common characteristics of silicon wafers, including polished wafers as well as substrates for epitaxial and certain other kinds of silicon wafers.

2 Scope

2.1 These specifications cover ordering information and certain requirements for high-purity (electronic grade), single crystal polished silicon wafers used in semiconductor device and integrated circuit manufacturing. Such wafers are usually sliced from cylindrical single-crystal ingots that have been ground to a uniform diameter prior to slicing. These specifications also cover ordering information and certain requirements for electronic grade silicon wafers intended for use as substrates (or starting wafers) for other kinds of wafers, including epitaxial, annealed, and SOI wafers.

2.2 Dimensional requirements are provided for the following categories of polished wafers:

- Category 1.1 2 inch polished single crystal silicon wafers with secondary flat
- Category 1.2 3 inch polished single crystal silicon wafers with secondary flat
- Category 1.5 100 mm polished single crystal silicon wafers, 525 μm thick, with secondary flat
- Category 1.6 100 mm polished single crystal silicon wafers, 625 μm thick, with secondary flat
- Category 1.7 125 mm polished single crystal silicon wafers with secondary flat
- Category 1.8.1 150 mm polished single crystal silicon wafers with secondary flat and T/3 edge profile template
- Category 1.8.2 150 mm polished single crystal silicon wafers with secondary flat and T/4 edge profile template
- Category 1.9.1 200 mm notched polished single crystal silicon wafers with T/3 edge profile template
- Category 1.9.2 200 mm notched polished single crystal silicon wafers with T/4 edge profile template
- Category 1.9.3 200 mm notched polished single crystal silicon wafers with parameter-specified edge profile
- Category 1.10.1 200 mm flatted polished single crystal silicon wafers with T/3 edge profile template without secondary flat
- Category 1.10.2 200 mm flatted polished single crystal silicon wafers with T/4 edge profile template without secondary flat
- Category 1.11 100 mm flatted polished single crystal silicon wafers without secondary flat
- Category 1.12 125 mm flatted polished single crystal silicon wafers without secondary flat

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- Category 1.13.1 150 mm flatted polished single crystal silicon wafers with T/3 edge profile template without secondary flat
- Category 1.13.2 150 mm flatted polished single crystal silicon wafers with T/4 edge profile template without secondary flat
- Category 1.15 300 mm notched polished single crystal silicon wafers with T/4 edge profile template
- Category 1.15.1 300 mm notched polished single crystal silicon wafers with parameter-specified edge profile
- Category 1.16.1 450 mm polished single crystal silicon wafers with notch centered on <110> axis
- Category 1.16.2 450 mm polished single crystal silicon wafers with notch centered on <100> axis

2.2.1 Values given for thickness, total thickness variation (TTV), bow, and warp apply only to wafers prior to application of back surface films, extrinsic gettering treatments, or other thermal treatments.

2.2.2 The dimensional characteristics of Category 1.10.1, 1.10.2, 1.11, 1.12, 1.13.1, and 1.13.2 wafers specified in this document are identical with those specified in JEITA EM-3602, and the dimensional characteristics of Category 1.15 wafers are essentially equivalent with those specified in JEITA EM-3602.

2.3 A complete purchase specification requires that additional physical properties be specified along with test methods suitable for determining their magnitude. This Standard provides a comprehensive listing of such properties and associated test methods. This listing provides a systematic basis for constructing the purchase specification for any kind of polished silicon wafer or substrate and is expected to be used for such purposes.

2.4 These specifications apply specifically to prime silicon wafers with at least one chem-mechanically polished surface. Ground, lapped, and unpolished wafers are not covered in this Specification but this Specification may provide guidance in connection with their procurement.

~~2.5 In addition, these specifications cover specification requirements for basic 300 mm diameter, double-side polished silicon wafers that are suitable for many advanced integrated circuit applications. If this kind of wafer is desired, physical properties other than those listed in the table of requirements shall not be included in the purchase specification.~~

~~2.6~~ 2.5 This Standard also provides guides for the specification of 300 and 450 mm diameter prime silicon wafers for the 32, 22, and 16 nm technology generations. These are included in Related Information 1.

~~2.7~~ 2.6 These specifications do not cover the requirements for the following related silicon materials and wafers:

- Polycrystalline silicon (see SEMI M16 or JEITA EM-3601A),
- Epitaxial wafers (see SEMI M62),
- Epitaxial wafers with buried layer (see SEMI M61),
- Test wafers (see SEMI M8),
- Premium wafers (see SEMI M24),
- Reclaimed wafers (see SEMI M38),
- Annealed wafers (see SEMI M57),
- SOI wafers (see SEMI M41, SEMI ~~M77~~M71, or JEITA EM-3603B), and

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- Solar-grade silicon wafers (see SEMI ~~M6~~PV22).

They do, however, provide the ordering information for test, premium, and reclaimed wafers, as well as the ordering information for the polished substrates and starting wafers used to prepare epitaxial, annealed, and SOI wafers.

~~2.8~~ 2.7 For referee purposes, U.S. customary units shall be used for wafers of 2 inch and 3 inch nominal diameters, and SI (system international, commonly called metric) units for 100 mm and larger diameter wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

~~SEMI M6 — Specification for Silicon Wafers for Use as Photovoltaic Solar Cells~~

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M16 — Specification for Polycrystalline Silicon

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M26 — Guide for the Re-Use of 100, 125, 150, and 200 mm Wafer Shipping Boxes Used to Transport Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Silicon Wafers

SEMI M41 — Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide to Conversion Factors for Interstitial Oxygen in Silicon

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Reference Spheres on Unpatterned Semiconductor Wafer Surfaces

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SEMI M57 — Guide for Specifying Silicon Annealed Wafers

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI M61 — Specification for Silicon Epitaxial Wafers with Buried Layers

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI M67 — Practice for Determining Wafer Near-Edge Geometry from a Measured Thickness Data Array Using the ESFQR, ESFQD and ESBIR Metrics

SEMI M68 — Practice for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD

SEMI M70 — Practice for Determining Wafer-Near-Edge Geometry Using Partial Wafer Site Flatness

SEMI M71 — Specification for Silicon-on-Insulator (SOI) Wafers for CMOS LSI

SEMI M73 — Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles

SEMI M77 — Practice for Determining Wafer Near-edge Geometry Using Roll-Off Amount, ROA

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF28 — Test Methods for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductive Decay

SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF391 — Test Methods for Minority Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF533 — Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 —Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

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SEMI MF847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF978 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1048 — Test Method for Measuring Reflective Total Integrated Scatter

SEMI MF1049 — Practice for Shallow Etch Pit Detection on Silicon Wafers

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1239 — Test Method for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1528 — Test Method for Measuring Boron Contamination in Heavily Doped *n*-Type Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with *p*-Polarized Radiation Incident at the Brewster Angle

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

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SEMI MF1982 — Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI PV22 — Specification for Silicon Wafers for Use in Photovoltaic Solar Cells

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-sided Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standards*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

ASTM D523 — Standard Test Method for Specular Gloss

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

3.4 *DIN Standards*[3]

3.5 *European Community Directive*[4]

2002/95/EC — On the restriction of the use of certain hazardous substances in electrical and electronic equipment

3.6 *ISO Standard*[5]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

3.7 *JEITA Standards*[6]

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

JEITA EM-3501 — Standard Methods for Determining the Orientation of a Semiconductor Silicon Single Crystal

JEITA EM-3502 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

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[1] American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287. New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023; http://www.ansi.org

[2] American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; http://www.astm.org

[3] Deutches Institut für Normung e.V., silicon standards are no longer available in either English and German editions from Beuth Verlag GmbH, Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601-0; Fax: 49.30.2601.1263; http://www.beuth.de. Consequently these standards have been removed from this section and moved to a Related Documents section at the end ~~of the text~~ of this standard.

[4] *Official Journal of the European Union*, February 13, 2003 Available for downloading from the following URL: http://164.36.164.20/sustainability/pdfs/finalrohs.pdf

[5] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; http://www.iso.ch

[6] Japanese Electronic and Information Technology Industries Association, 3rd Fl., Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan. http://www.jeita.or.jp

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JEITA EM-3503 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

JEITA EM-3504 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

JEITA EM-3508 — Test Method for Bulk Micro Defect Density and Denuded Zone Width in Annealed Silicon Wafers

JEITA EM-3601A — Standard Specification for High Purity Polycrystalline Silicon

JEITA EM-3602 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surfaces

JEITA EM-3603B — Standard of SOI Wafers and Metrology

3.8 *JIS Standards*[7]

JIS H 0604 — Measuring of Minority-carrier Lifetime in Silicon Single Crystal by Photoconductive Decay Method

JIS H 0607 — Determination of Conductivity Type in Germanium by Thermoelectromotive Method

JIS H 0609 — Test methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

JIS H 0615 — Test Method for Determination of Impurity Concentrations in Silicon Crystal by Photoluminescence Spectroscopy

JIS Z 8741 — Specular Glossiness – Methods of Measurement

3.9 *MHIA Standard*[8]

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items. These items are indicated on the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, shown in Table 1, with a ♦ symbol in the left-most column.

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation

[7] Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014; http://www.jsa.or.jp

[8] Material Handling Industry of America (MHIA), 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA. Telephone: 704.676.1190; Fax: 704.676.1199; http//www.mhia.org

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- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary Flat Length
- 2-6.5 Secondary Flat Location
- 2-6.6 Edge profile
- 2-6.7 Thickness

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures,

5.3.2 Certification (if required) and

5.3.3 Packing and shipping container labeling requirements.

5.4 Finally, many other characteristics may also be specified in purchase orders for silicon wafers. These shall be selected from the other items listed in the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2 (see Table 1).

5.5 The parameter values provided in the requirements tables in § 6 may be used to identify appropriate values in the specification without selecting a value for each line. However, even if these requirements table values are used, the desired test methodology must be selected in accordance with ¶ 5.2.

5.6 It is essential that all choices for the items selected to be specified be made in order not to have unspecified parameters that would lead to surprises between supplier and customer. This is particularly important in the specification of wafer site flatness, for which a variety of parameters must be selected as outlined in Appendix 1.

5.7 Of the various items listed, the following (listed in the order in which they appear in Table 1) are most often selected, especially for wafers to be used for advanced integrated circuit manufacture:

- 2-1.6 Nominal edge exclusion (to define the fixed quality area (FQA), see Figure 1.)
- 2-4 Structural characteristics
- 2-5.1 Wafer ID Marking
- 2-6.6 Edge Profile
- 2-6.8 Total Thickness Variation (TTV or GBIR, see ¶ ~~R2~~R4-7.7)
- 2-6.10 Warp (and sometimes 2-6.9 Bow or 2-6.11 Sori)
- 2-6.13 Site Flatness (SFQR)
- 2-8.5 Localized Light Scatterers (LLS)

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Table 1 Silicon Wafer Specification Format for Order Entry, Parts 1 and 2

Part 1 General Information

ITEM	*INFORMATION*	*Date:*
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2 Polished Wafer or Substrate

		ITEM	*SPECIFICATION*	*MEASUREMENT METHOD*
2-1 GENERAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.)*				
♦	2-1.1	Growth Method	[ ] Cz; [ ] FZ; [ ] MCz; [ ] Supplier option of Cz or MCz	
	2-1.2	Use of Refined Polysilicon	[ ] Permitted; [ ] Not permitted	
♦	2-1.3	Crystal Orientation	[ ] (100); [ ] (111); [ ] (110); [ ] Other: (specify) ( )	[ ] SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ] JEITA EM-3501; [ ] Other: (specify)_____
♦	2-1.4	Conductivity Type	[ ] *p;* [ ] *n*	[ ] SEMI MF42; [ ] JIS H 0607; [ ] Other: (specify)_____
♦	2-1.5	Dopant	[ ] B; [ ] P; [ ] Sb; [ ] As; [ ] Neutron Transmutation Doped; [ ] Other: (specify) _____	
	2-1.6	Nominal Edge Exclusion[#1] (see Figure 1)	[ ] 2 mm; [ ] 3 mm; [ ] 5 mm; [ ] Other: (specify)_____mm	
	2-1.7	Co-dopant in Crystal	[ ] None; [ ] Nitrogen; [ ] Carbon; [ ] Nitrogen and Carbon; [ ] Argon; [ ] Other: (specify)_____	
♦	2-1.8	Wafer Surface Orientation (with respect to crystal orientation, see item 2-1.3)	[ ] On-orientation: [ ] 0.00° ± 1.00°; [ ] 0.00° ± ____° [ ] Off-orientation: [ ] 0.6° ± 0.4° [ ] 2.50° ± 0.50°; [ ] 4.00° ± 0.50°; [ ] _____° ± _____°	[ ] SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ] JEITA EM-3501; [ ] Other: (specify)_____
	2-1.9	Orthogonal Misorientation (see Figure 2)	[ ] ±5° max; [ ] Other: ±[ ]°, max	
2-2 ELECTRICAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.)*				
♦	2-2.1	Resistivity Measured at	Nominal [ ] ± Tolerance [ ] Ω·cm [ ] Center Point; [ ] Other: (specify)_____	[ ] SEMI MF84; [ ] SEMI MF673; [ ] Other: (specify)_____
	2-2.2	Radial Resistivity Variation (RRG)	Not greater than [ ]%	SEMI MF81 Figure 1 – [ ] A, [ ] B, [ ] C, [ ] D; [ ] DIN 50435; [ ] Other: (specify) _____
	2-2.3	Resistivity Striations	Not greater than [ ]%	[ ] SEMI MF525; [ ] Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
	2-2.4	Minority Carrier Lifetime	Greater than [ ] μs	SEMI MF28 [ ] A, [ ] B; SEMI MF391 [ ] A, [ ] B; [ ] SEMI MF1388; [ ] SEMI MF1535; [ ] JEITA EM-3502; [ ] JIS H 0604; [ ] Other: (specify)_____
2-3 CHEMICAL CHARACTERISTICS				
	2-3.1	Oxygen Concentration (Values using the following Calibration Factor, see SEMI M44)	Nominal [ ] ± Tolerance [ ]; [ ] × 10^{17} cm^{-3}; [ ] ppma [ ] IOC-88; [ ] Old ASTM; [ ] New ASTM or DIN; [ ] Original JEITA; [ ] Other: (specify)_____	IR (Interstitial): [ ] SEMI MF1188; [ ] SEMI MF1619; [ ] JEIDA EM-3504; [ ] Other: (specify)_____ [ ] SIMS (Total): SEMI MF1366; [ ] GFA (Total)
	2-3.2	Radial Oxygen Variation	Not greater than [ ]%	SEMI MF951 Plan [ ] A1; [ ] A2; [ ] A3; [ ] B; [ ] B1; [ ] C; [ ] D; [ ] Other: (specify)_____
	2-3.3	Carbon Concentration (Background, cf. 2-1.7)	Not greater than [ ] [ ] ppma; [ ] × $10^{16}$$cm^{-3}$	[ ] SEMI MF1391; [ ] JEITA EM-3503; [ ] Other: (specify)_____
	2-3.4	Boron Concentration in Heavily Doped *n*-type Silicon	Not greater than [ ] ppba	[ ] SEMI MF1528; [ ] Other: (specify)_____
	2-3.5	Bulk Iron Content	[ ] Not greater than [ ] × $10^{[\ ]}$ $atoms/cm^3$	[ ] SEMI MF978 (DLTS); [ ] SEMI MF391(SPV); [ ] SEMI MF1535; [ ] JEITA EM3502 (μτ); [ ] Other (specify): _____
	2-3.6	Hazardous Substances Restrictions	[ ] EC Directive 2002/95/EC [ ] Other: (specify) _____	Specify: _____ (see Appendix 2)
2-4 STRUCTURAL CHARACTERISTICS				
	2-4.1	Dislocation Etch Pit Density	[ ] Not greater than [ ]/cm^2	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.2	Slip	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.3	Lineage	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.4	Twin Boundary	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.5	Swirl	[ ] Not greater than [ ]% of wafer area	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.6	Shallow Pits	Not greater than [ ]/cm^2	[ ] SEMI MF1727; [ ] SEMI MF1049; [ ] Other: (specify)_____
	2-4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than [ ]/cm^2	Test Cycle: [ ] SEMI MF1727; [ ] JIS H 0609; [ ] Other: (specify)_____ Observation Method: [ ] SEMI MF1726; [ ] JIS H 0609; [ ] Other: (specify)_____

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		ITEM	SPECIFICATION	MEASUREMENT METHOD
	2-4.8	Oxide Precipitates	Range: [ ] to [ ] Unit: [ ] cm^{-2}; [ ] cm^{-3}	Test Cycle: SEMI MF1239 [ ] A, [ ] B; [ ] Other: (specify)_____
	2-4.9	Interstitial Oxygen Reduction ($\Delta[O_i]$)	Range: [ ] to [ ] [ ] ppma; [ ] × 10^{17} cm^{-3}	Test Cycle: SEMI MF1239 [ ] A, [ ] B; [ ] Other: (specify)_____
	2-4.10	Bulk defects by X-ray topography	[ ] Density:_____ cm^{-3}	[ ] Specify_____
2-5 WAFER PREPARATION CHARACTERISTICS				
	2-5.1	Wafer ID Marking	[ ] None; [ ] SEMI M12; [ ] SEMI M13; [ ] SEMI T1; [ ] SEMI T2; [ ] SEMI T7; [ ] SEMI T7 + optional alphanumeric mark (see Figure 3); [ ] Other: (specify) _____	
	2-5.2	Front Surface Thin Film(s)	[ ] None [ ] Description:	
	2-5.3	Denuded Zone	[ ] None [ ] Description:	
	2-5.4	Extrinsic Gettering	[ ] None [ ] Description:	
	2-5.5	Backseal	[ ] None [ ] Description:	
	2-5.6	Annealing	[ ] None [ ] Description:	
	2-5.7	Edge Surface Condition	[ ] Ground; [ ] Etched; [ ] Polished[#2]	
	2-5.8	Back Surface Condition	[ ] Supplier Option; [ ] Caustic Etched; [ ] Acid Etched; [ ] Polished[#2] (see Item 2-9.8 for required gloss level)	
2-6 DIMENSIONAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.* THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE [ ] Specified According to Category 1.__ Polished Wafers (see Tables ~~5–11~~3-9). If the items are specified according to a standard wafer Category, all the items specified in these tables ~~-~~need not be entered individually.					
♦➲	2-6.1	Diameter	[ ] Nominal [ ] ± Tolerance [ ] mm	[ ] SEMI MF2074; [ ] Other: (specify)_____
♦➲	2-6.2	Fiducial Dimensions	Flat [ ] Length or [ ] Diameter:[#3] [ ] Nominal [ ] ± Tolerance [ ] mm [ ] Notch Dimensions (see Figure 5)	[ ] SEMI MF671 (Flat Length); ~~[ ] Flat Diameter [#3] Specific method _____;~~ [ ] SEMI MF1152 (Notch Dimensions); [ ] Other: (specify)_____
♦➲	2-6.3	Primary Flat/Notch Orientation	[ ] (crystal axis) [_____] ± ____°	[ ] SEMI MF847 (Flat); [ ] Other: (specify)_____
♦➲	2-6.4	Secondary Flat Length	[ ] None; [ ] Other: _____±____mm	[ ] SEMI MF671; [ ] Other: (specify)_____
♦➲	2-6.5	Secondary Flat Location (see Figure 4)	[ ] None; [ ] Other: (θ) _____°	
♦➲	2-6.6	Template-Coordinate Based Edge Profile Specification	[ ] T/3 template [ ] T/4 template [ ] Other template (specify)_____	SEMI MF928: Method A [ ], Method B [ ]; [ ] Other: (specify)_____

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		ITEM	SPECIFICATION	MEASUREMENT METHOD
		Profile-Parameter-Based Edge Profile Specification	[ ] Front edge width ____µm ± ____µm [ ] Front bevel angle ____° ± ____° [ ] Front shoulder radius ____µm ± ___µm [ ] Back shoulder radius ____µm ± ___µm [ ] Back bevel angle ____° ± ____° [ ] Back edge width ____µm ± ___µm [ ] Front apex length ____µm ± ___µm (optional) #4 [ ] Back apex length ____µm ± ___µm (optional) #4 [ ] Front apex angle ____° ± ____° (optional) #4 [ ] Back apex angle ____° ± ____° (optional) #4	SEMI M73:#5 Method 1 [ ], Method 2 [ ]; ~~[ ] Target profile-based template of width ____ µm;~~ [ ] Other: (specify)_____
♦ ➲	2-6.7	Thickness	[ ] Nominal [ ] ± Tolerance [ ] µm	[ ] SEMI MF533; [ ] SEMI MF1530; [ ] JIS H 0611; [ ] Other: (specify)_____
➲	2-6.8	Total Thickness Variation (TTV)	[ ] [ ] µm, max.	[ ] SEMI MF533; [ ] JIS H 0611; [ ] SEMI MF657 (partial scan); [ ] SEMI MF1530 (full scan); [ ] Other: (specify)_____
➲	2-6.9	Bow	[ ] [ ] µm, max	[ ] SEMI MF534; [ ] JIS H 0611; [ ] Other: (specify)_____
➲	2-6.10	Warp	[ ] [ ] µm, max	[ ] SEMI MF657; [ ] SEMI MF1390; [ ] Other: (specify)_____
	2-6.11	Sori	[ ] [ ] µm, max	[ ] SEMI MF1451; [ ] JEITA EM-3401; [ ] Other: (specify)_____
	2-6.12	Flatness, Global	Acronym:~~#4#6~~ [ ] [ ] [ ] [ ] [ ] Value: [ ]µm	[ ] SEMI MF1530; [ ] JEITA EM-3401; [ ] Other: (specify)_____
	2-6.13	Flatness, Site	Acronym:~~#4#6~~ [ ] [ ] [ ] [ ] [ ] Value: Not greater than [ ] µm; Site Size ___ mm × ___ mm [ ]% Usable Area_____ [ ] Include partial sites; [ ] Do not include partial sites; Offset: x = [ ] mm, y = [ ] mm	[ ] SEMI MF1530; [ ] Other: (specify)_____
	2-6.14	Nanotopography	[ ] SEMI M43 (specify conditions):_____	
	2-6.15	Near Edge Geometry	[ ] ESFQR, [ ] ESFQD. or [ ] ESBIR [ ] ZDD [ ] L-ROA, [ ] P-LOA [ ] PSFQR, [ ] PSFQD	SEMI M67 SEMI M68 SEMI M77 SEMI M70
2-7 FRONT SURFACE CHEMISTRY				
	2-7.1	Surface Metal Contamination		
	2-7.1.1	Sodium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____
	2-7.1.2	Aluminum	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
	2-7.1.3	Potassium	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.4	Chromium	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.5	Iron	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.6	Nickel	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.7	Copper	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.8	Zinc	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.1.9	Calcium	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.2	Other Surface Metals (List Separately)		
	2-7.2.1	_____	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.2.2	_____	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.2.3	_____	[ ] Not greater than [ ] × $10^{[ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
	2-7.2.4	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.2.5	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.2.6	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ] ICP/MS; [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] SEMI M33 (TXRF); [ ] ISO 14706 (TXRF); [ ] Other: (specify)_____
	2-7.3	Surface Organics	[ ] Not greater than [ ]ng/cm^2	[ ] SEMI MF1982; [ ] Other: (specify)_____
2-8 FRONT SURFACE INSPECTION CHARACTERISTICS FOR ALL WAFER DIAMETERS, THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY. ALTERNATIVELY, FOR WAFERS 150 mm OR LESS IN DIAMETER, WHICH CAN BE INSPECTED VISUALLY, THE ITEMS LISTED MAY BE [ ] Specified according to Table 12. If the items are specified according to Table 12, the items marked with the symbol ⩛ need not be entered individually.				
⩛	2-8.1	Scratches – Macro	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.2	Scratches – Micro	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.3	Pits	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.4	Haze	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.5	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.6	Contamination/Area	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.7	Edge Chips and Indents	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____
⩛	2-8.8	Edge Cracks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#5#7] [ ] Other: (specify)_____

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		ITEM	SPECIFICATION	MEASUREMENT METHOD
✓	2-8.9	Cracks, Crow's Feet	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.10	Craters	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.11	Dimples	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.12	Grooves	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.13	Mounds	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.14	Orange Peel	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
✓	2-8.15	Saw Marks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;~~#5~~#7 [ ] Other: (specify)_____
	2-8.16	Dopant Striation Rings	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-8.17	Stains	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-8.18	rms Microroughness	[ ] Not greater than [ ] nm, over spectral range from [ ] μm^{-1} to [ ] μm^{-1}	[ ] SEMI MF1048; [ ] AFM; [ ] Other (specify)_____
2-9 BACK SURFACE INSPECTION CHARACTERISTICS				
			FOR ALL WAFER DIAMETERS, THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY. ALTERNATIVELY, FOR WAFERS 150 mm OR LESS IN DIAMETER, WHICH CAN BE INSPECTED VISUALLY, THE ITEMS LISTED MAY BE [ ] Specified according to Table 12. If the items are specified according to Table 12, the items marked with the symbol ✓ need not be entered individually.	
✓	2-9.1	Edge Chips	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.2	Edge Cracks	[ ] None; [ ] Other (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.3	Cracks, Crow's Feet	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.4	Contamination/Area	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.5	Saw Marks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.6	Stains	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.7	Roughness	[ ] _____ nm rms	[ ] SEMI M40; [ ] Other: (specify)_____
	2-9.8	Brightness (Gloss)	[ ] _____	[ ] ASTM D 523; [ ] JIS Z 8741; [ ] Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	2-9.9	Scratches – Macro	[ ] None; [ ] Cum Length =[ ] mm	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.10	Scratches – Micro	[ ] None; [ ] Cum Length =[ ] mm	[ ] SEMI MF 523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.11	Localized Light Scatterers	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS~~#6~~#7; [ ] Other: (specify)_____
2-10 OTHER (as required)				

#1 The nominal edge exclusion, *EE*, specifies the diameter of the FQA, which is given by the nominal diameter (see Item 2-6.1) minus 2*EE* (see Figure 1). This quantity provides a center referenced property. Although use of edge referenced properties is discouraged, some equipments and procedures are based on edge referenced dimensions. When this occurs, the quality area is not fixed and some part of the fixed quality area may fall outside the evaluated area, which is generally not a desirable situation.

#2 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

#3 Note that in the case of {100} *n*-type wafers, 125 mm or smaller in diameter, with a secondary flat (Categories 1.1, 1.2, 1.5, 1.6, and 1.7) the primary and secondary flats are opposing and the concept of flat diameter does not apply because the diameter perpendicular to the flats does not intersect the wafer circumference.

#4 See the discussion in ¶ 6.6.3.2.2 and following paragraphs for cautions if these parameters are specified.

#5 Thickness reported by parameter based edge profile measurement is typically different from the actual wafer thickness reported by standard dimensional metrology equipment used for flatness and shape. This is due to limitations imposed by the edge profile technique. Users are cautioned not to assume the edge profile reported thickness is a valid wafer dimension.

~~#4~~#6 Flatness Acronyms are defined in the Flatness Decision Tree in Appendix 1.

~~#5~~#7 In today's technology, it may be possible to inspect for some of these items using automated surface scanning inspection systems (SSIS). Such systems should be calibrated according to SEMI M53 using polystyrene latex spheres deposited in accordance with SEMI M58. Some indication of the defects separable by such instruments is provided in SEMI M35; however, a standard test procedure has yet to be developed. Application of automated inspection with the use of an SSIS must be agreed upon between supplier and customer.

6 Requirements

6.1 *General Characteristics*

6.1.1 The crystal growth method shall be modified Czochralski (Cz), float zone (FZ), or magnetic Czochralski (MCz) as specified on the purchase order. In some cases, the supplier is given the option of selecting Cz or MCz.

6.1.1.1 If the Cz or MCz method is used for crystal growth, it may be permissible to utilize refined (previously melted) polysilicon in the growth charge; when this is the case, the appropriate box should be checked.

6.1.2 The crystal orientation shall be as specified on the purchase order. Usually either (100) or (111) is specified, but (110) is sometimes specified for polished wafers to be used for making SOI wafers. Occasionally, another orientation, such as (311) or (511), is specified.

6.1.3 The conductivity type shall be either *n* or *p*.

6.1.4 The dopant shall be specified to match the conductivity type. In general, boron (B) is used for *p*-type material, while phosphorus (P) is most commonly used for *n*-type material. For some applications, antimony (Sb) or arsenic (As) are used to obtain *n*-type wafers. For high power applications, neutron transmutation doping is often used to obtain high resistivity *n*-type wafers.

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6.1.5 The nominal edge exclusion, *EE*, specifies the diameter of the fixed quality area (FQA), which is given by the nominal diameter minus 2·*EE* (see Figure 1). The fixed quality area is a center-referenced region that is independent in size from the tolerances of both wafer diameter and flat length. For the purposes of defining the FQA, the periphery of a wafer of nominal dimensions at a location with a notch is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter.

6.1.5.1 The nominal edge exclusion is usually specified as 2 mm or 3 mm, but some advanced wafer processing technologies are moving in the direction of 1 mm. However, it should be noted that not all processes and metrology can work as close to the wafer edge as implied by the nominal edge exclusion.

6.1.5.2 In addition, it is sometimes necessary to specify additional exclusion zones, such as those for wafer identification marks or wafer holding areas.

6.1.5.3 Although use of edge-referenced properties is discouraged, some equipments and procedures are based on edge referenced dimensions. When this occurs, the quality area is not fixed and some part of the fixed quality area may fall outside the evaluated area, which is generally not a desirable situation.

6.1.6 A co-dopant may be required for polished wafers intended to be processed into annealed wafers. Some co-dopants may also be used in connection with control of oxygen precipitation characteristics even when the wafer is not annealed.

6.1.7 *Wafer Surface Orientation* — The wafer shall conform to the surface orientation as specified in the purchase order.

6.1.7.1 For on-orientation wafers, the angular tolerance from the plane perpendicular to the growth axis shall be specified.

6.1.7.2 For off-orientation wafers, both the misorientation angle from the growth axis and its angular tolerance shall be specified.

6.1.7.2.1 A misorientation angle between 0.2° and 1° (0.6° ± 0.4°) from a (100) plane is frequently used for some epitaxial substrates.

6.1.7.2.2 A misorientation angle of 2.50° or 4° ± 0.5° from a (111) plane is often used for other epitaxial substrates.

6.1.7.3 Orthogonal misorientation is the tilt angle of the normal to a (111) wafer surface toward nearest <110> direction in a plane parallel with the primary flat as indicated in Figure 2.

6.1.7.3.1 The contribution of 5° of orthogonal misorientation to the total off-orientation angle is less than 0.5°.

6.1.7.4 For ion implant applications, the following tolerance issues should be considered:

6.1.7.4.1 For general use where channeling is to be avoided, the current wafer orientation specification of ±1.0° deviation from the [100] axis (perpendicular to the (100) plane of the wafer) is adequate. This Specification is suitable for minimum channeling applications, provided that the appropriate ion implant equipment angle settings are employed.

6.1.7.4.2 Uniform, maximum channeling along the [100] axis perpendicular to the (100) wafer surface is strongly dependent on strict adherence to a 0° tilt angle. To achieve maximum channeling, crystallography requires the orientation to be within ±0.1° of a <100> direction. Also, the customer must remove all overlying oxide, nitride, poly, etc., layers from the wafer prior to a channeling implant. The customer must maintain very rigid control of the ion implant equipment angle setting in order to achieve maximum channeling across the wafer.

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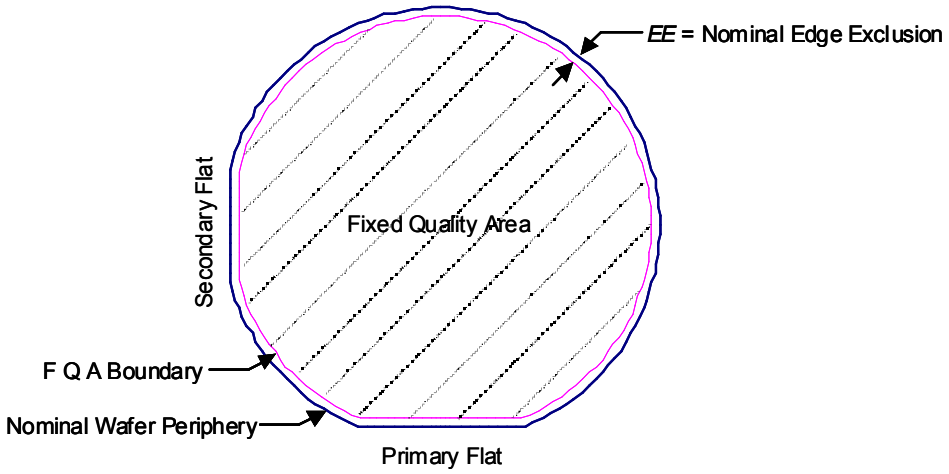
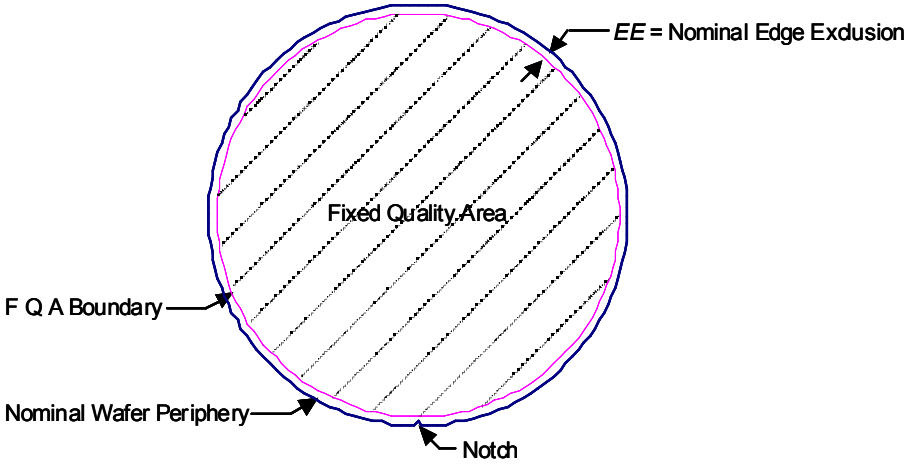
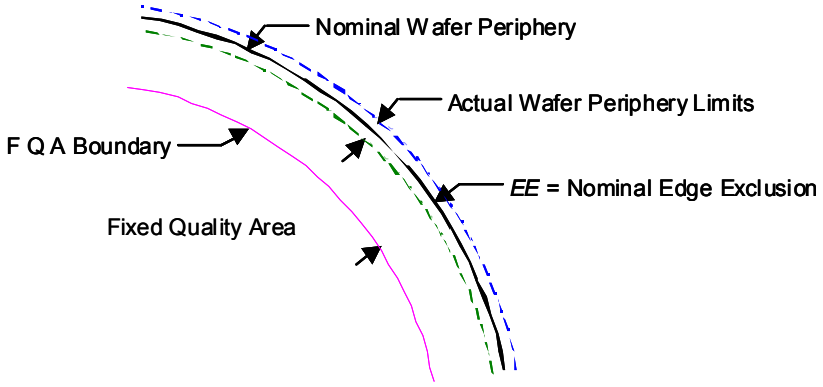


a. Flatted Wafer



b. Notched Wafer



c. Nominal and Actual Wafer Peripheries

Figure 1
Fixed Quality Area

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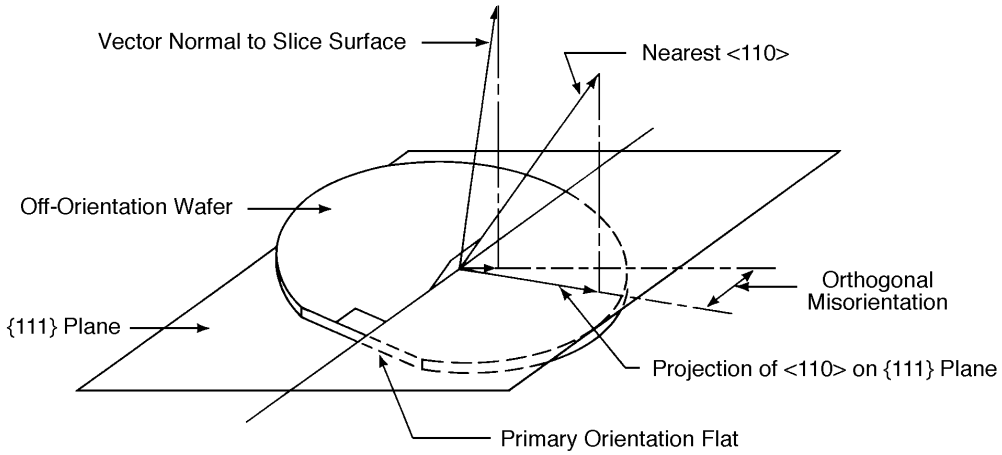

NOTE: If the off-orientation angle is determined with the seed end up, the polished surface of the finished wafer must be the surface toward the seed end, and vice versa. Polishing of the incorrect wafer surface results in an incorrect wafer tilt, which can cause unwanted pattern shifts and distortions if the wafer is used subsequently for epitaxial layer growth. Because the convention for determining the off-orientation angle is not the same worldwide, it is essential to establish accurately the desired convention.

Figure 2
Orthogonal Misorientation of {111} Wafer

Table 2 Energy Ranges for Ion Implant Modeling

Species	*Energy Range (keV)*
B	15 to 80
BF_2	15 to 65
As	15 to 180

6.1.7.5 The tolerance of ±0.1° is derived from experimental ion implant profile data and ion implant modeling activity for implants into (100) silicon wafers. The ranges for which data was obtained are given in Table 2.

6.2 *Electrical Characteristics*

6.2.1 The center-point room temperature resistivity of the wafers shall conform to the nominal and tolerance values specified on the purchase order.

6.2.2 The wafers shall conform to any requirements specified on the purchase order for radial resistivity variation, resistivity striations and minority carrier lifetime.

6.3 *Chemical Characteristics*

6.3.1 The wafers shall conform to any requirements specified on the purchase order for oxygen concentration, radial oxygen variation, carbon concentration, and, for heavily doped (low resistivity) *n*-type silicon wafers only, compensating boron concentration.

6.3.2 If specified on the purchase order, the wafers shall conform to the hazardous substances regulatory requirements of a jurisdiction. At present, the only publicly available requirements are in EC Directive 2002/95/EC. For information, the maximum concentrations of ~~*Cr, Cd, Hg,* and *Pb*~~ Cr, Cd, Hg, and Pb in the bulk or on the surface of the wafer required by this directive are given in Appendix 2.

NOTE 1: As requirements from other jurisdictions become publicly available, they will be added to Appendix 2.

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6.4 *Structural Characteristics*

6.4.1 The wafers shall conform to any requirements specified on the purchase order for dislocation etch pit density, slip, lineage, twin, swirl, shallow pits, oxidation induced stacking faults (OSF), oxide precipitates, interstitial oxygen reduction upon appropriate heat treatment, bulk defects by X-ray topography, and bulk microdefects (BMD).

6.5 *Wafer Preparation Characteristics*

6.5.1 *Wafer ID Marking* — Where wafer ID marking is specified on the purchase order, the kind of marking must be indicated.

6.5.1.1 Where alphanumeric marking is specified for wafers of 200 mm diameter and smaller, the code character properties and code field location shall conform either to SEMI M13 or to SEMI M12, as specified on the purchase order.

6.5.1.2 Where back-surface bar code marking is specified for wafers of 200 mm diameter and smaller, the code symbol and its location shall be agreed upon between supplier and customer.

6.5.1.3 Where two-dimensional matrix code marking is specified for wafers of 200 mm diameter and smaller, the code symbol and its location shall be agreed upon between supplier and customer.

6.5.1.4 All 300 mm diameter wafers (wafer categories 1.15 and 1.15.1, see Table ~~10~~ 8) shall be marked with a two-dimensional matrix code symbol on the back surface outside the fixed quality area as soon after slicing as practical in the manner specified in SEMI T7 in order to provide both identification of these wafers and traceability of each wafer back to the ingot from which it was cut. The back surface is identified as the wafer surface with the two-dimensional matrix code symbol.

6.5.1.4.1 Optionally, the user may specify an additional back-surface mark as shown in Figure 3. This mark contains alphanumeric characters with:

- The same message characters as the SEMI T7 mark and appropriate checksum characters as defined by SEMI M12 and
- Character string as specified in SEMI M12.

NOTE 2: It is expected that this optional alphanumeric mark will not be used after users have developed successful experience with SEMI T7 mark usage.

6.5.1.4.2 Single density dot matrix, 5 dots horizontal and 9 dots vertical, shall be used.

6.5.1.4.3 Dot diameter shall be the same as that used for the two-dimensional matrix code symbol (see ¶ 6.5.1.4).

6.5.1.4.4 Character dimensions shall be as defined in Table 1 of SEMI M12 (nominal spacing = 1.42 mm, nominal width = 0.812 mm, nominal height = 1.624 mm).

6.5.1.4.5 Mark location (center of bottommost dot rows) relative to the reference point of the SEMI T7 mark shall be 1.40 ± 0.05 mm toward the wafer center, as shown in Figure 3.

6.5.1.4.6 Mark field height, as defined by the distance between the centers of the topmost and bottommost dot rows of the A/N characters, shall be 1.62 ± 0.03 mm (see Note 3).

6.5.1.4.7 Mark field length, as defined by the distance between the centers of the leftmost and rightmost dot columns of the A/N characters, shall be 16.43 ± 0.07 mm.

6.5.1.4.8 The mark-field shall be centered on the radius that passes through the reference point of the SEMI T7 mark as shown in Figure 3.

6.5.1.4.9 Character baseline shall be toward wafer OD and parallel with the row of the SEMI T7 mark that contains that mark's reference point.

NOTE 3: The overall length tolerance of the A/N mark is more stringent than that in SEMI M12. Also the height tolerance of the overall mark imposes tighter skew and offset tolerances than are required in SEMI M12.

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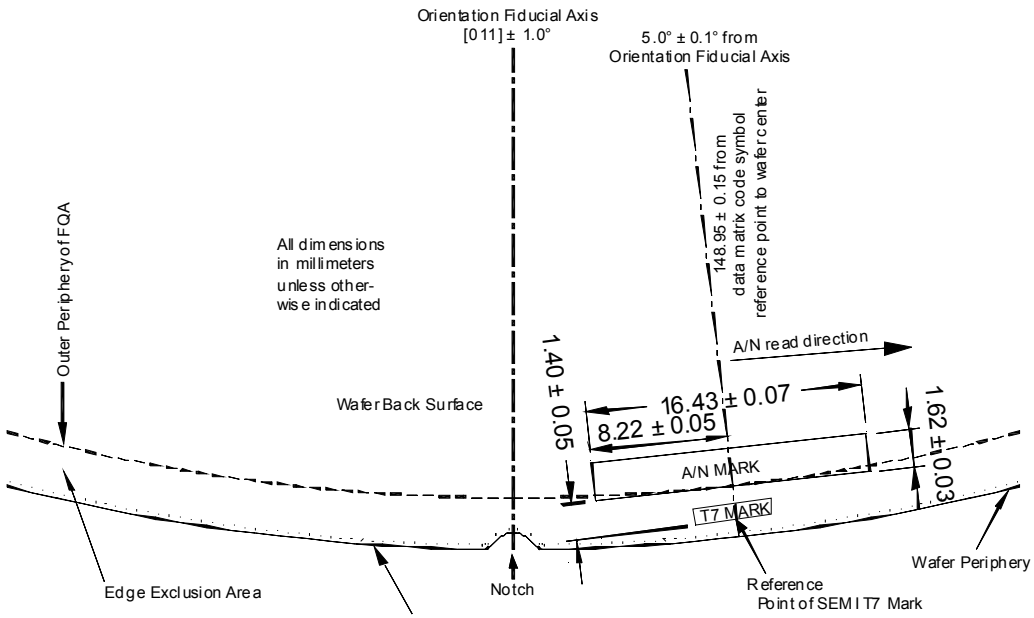

NOTE: A/N mark field dimensions are defined by the centers of the topmost and bottommost dot rows and the center of the leftmost and rightmost dot columns of the A/N characters. The field dimensions are more tightly controlled than those of a field constructed using SEMI M12. This results from the availability of laser marking capabilities not available when SEMI M12 was developed. In addition, the tolerance on the field dimensions is not cumulative.

Figure 3
Optional A/N Code Field Location on Back Surface of Notched 300 mm Diameter Wafer (~~Category~~ Categories 1.15 and 1.15.1)

6.5.2 *Other* — The wafers shall conform to any requirements specified on the purchase order for any other wafer preparation characteristics including front surface thin films, denuded zone, extrinsic gettering, backseal, annealing, and edge and back surface conditions.

6.6 *Dimensional Characteristics*

6.6.1 *Standard Wafer Categories* — The standardized dimensions, dimensional tolerances, and fiducial (flat or notch) characteristics for various standard wafer categories (see ¶ 2.2 for the wafer categories covered by this Standard) are summarized in Tables 3 through 9. These categories of wafers shall meet all requirements listed in the appropriate table, unless an exception is negotiated between supplier and customer and is shown on the purchase order.

NOTE 4: Based upon our experience with 300 mm wafers, Table 9 for 450 mm wafers contains many more standardized parameters than the tables for 300 mm and smaller wafers.

NOTE 5: Wafers of the same nominal diameter may typically have different dimensional configurations in different regions of the world. Many of these configurations are represented in these tables. In selecting the appropriate standard polished wafer category, consideration should be given to compatibility with processes and equipment generally available in the region of use.

~~6.6.1~~ 6.6.2 *Dimensions and Fiducials* — The wafers shall conform to the dimensions, dimensional tolerances, and fiducial (flat or notch) characteristics and locations as specified in the purchase order.

~~6.6.1.1~~ 6.6.2.1 Where secondary flats are specified, they shall be located as shown in Figure 4.

~~6.6.1.2~~ 6.6.2.2 Where notches are specified, they shall conform to the dimensions in Figure 5.

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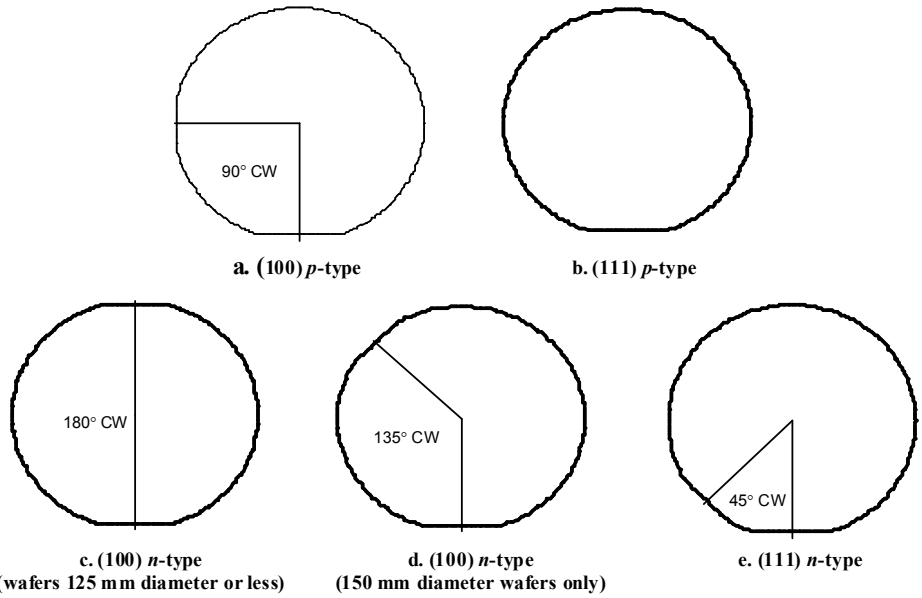


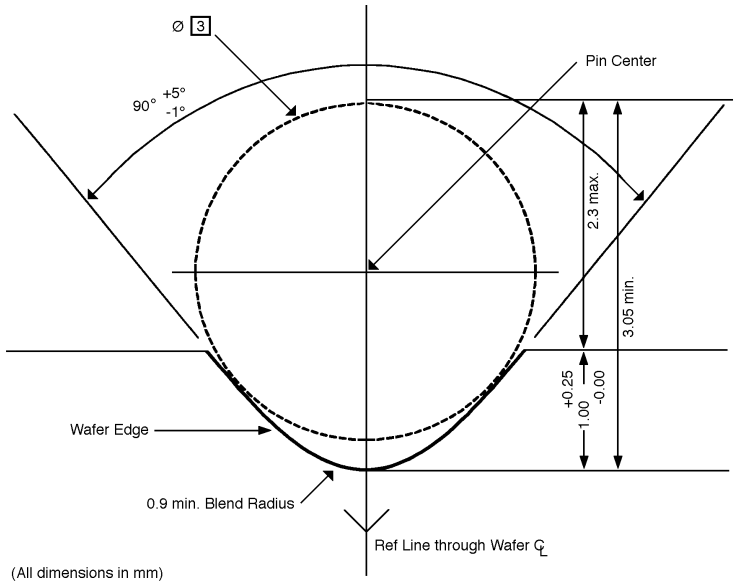
a. (100) *p*-type **b. (111) *p*-type**

c. (100) *n*-type (wafers 125 mm diameter or less) **d. (100) *n*-type (150 mm diameter wafers only)** **e. (111) *n*-type**

NOTE 1: Secondary flat location for 150 mm diameter (100) *n*-type wafers changed from configuration c to configuration d effective January 1, 1990.

NOTE 2: The angular position of the center point of the secondary flat is given in Table ~~5~~ 3 through Table ~~7~~ 5 both in terms of the clockwise angle from the primary flat, located at the bottom of each figure, to the secondary flat and the angle, θ, from the positive x-axis of the wafer coordinate system as defined by SEMI M20 (at 3 o'clock) to the secondary flat.

Figure 4
Secondary Flat Locations



NOTE: The pin shown in the outline on this figure is used to align the notched wafer in a fixture during use. The pin is also used to reference the notched wafer during testing for notch dimensions and dimensional tolerances. The notch dimensions shown in the figure assume a 3 mm diameter for this alignment pin.

Figure 5
Notch Dimensions

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Table 3 Dimensional Characteristics of 2 inch and 3 inch Polished Single Crystal Silicon Wafers[#1]

Property		*2 inch Wafers U.S. Customary[#2] Metric (SI)[#2]*		*3 inch Wafers U.S. Customary[#2] Metric (SI)[#2]*	
Previous SEMI Reference:		*SEMI M1.1*		*SEMI M1.2*	
Wafer Category:		*1.1*		*1.2*	
2-6.1	Diameter	2.000 ± 0.015 in.	50.80 ± 0.38 mm	3.000 ± 0.025 in.	76.20 ± 0.63 mm
2-6.2	Primary Flat Length	0.625 ± 0.065 in.	15.88 ± 1.65 mm	0.875 ± 0.125 in.	22.22 ± 3.17 mm
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°			
2-6.4	Secondary Flat Length	0.315 ± 0.065 in.	8.00 ± 1.65 mm	0.440 ± 0.060 in.	11.18 ± 1.52 mm
2-6.5	Secondary Flat Location (see Figure 4) {111} *p*-type {100} *p*-type {111} *n*-type {100} *n*-type	No secondary flat 90° ± 5° clockwise from primary flat (θ = 180° ± 5°) 45° ± 5° clockwise from primary flat (θ = 225° ± 5°) 180° ± 5° from primary flat (θ = 90° ± 5°)			
2.6.6	Edge Profile Coordinate, C_y (T/3 Template, see Table ~~3~~ 10)	0.0037 in.	93 µm	0.0050 in.	127 µm
2-6.7	Thickness, Center Point	0.0110 ± 0.0010 in.	279 ± 25 µm	0.0150 ± 0.0010 in.	381 ± 25 µm
2-6.8	Total Thickness Variation, Max.	0.0005 in.	12 µm	0.0010 in.	25 µm
2-6.9	Bow, Max.	0.0015 in.	38 µm	0.0016 in.	40 µm
2-6.10	Warp, Max.	not specified		0.0016 in.	40 µm

#1 Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.~~4~~1).

#2 For referee purposes, U.S. Customary units apply. To ensure that product shipped is within specification, any conversion to metric (SI) equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If the metric (SI) equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#3 For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

Table 4 Dimensional Characteristics of 100 mm and 125 mm Polished Single Crystal Silicon Wafers with Secondary Flat[#1]

Property		*100 mm Wafers (t=525µm)[#2]*	*100 mm Wafers (t=625µm)[#2]*	*125 mm Wafers[#2]*
Previous SEMI Reference:		*SEMI M1.5*	*SEMI M1.6*	*SEMI M1.7*
Wafer Category:		*1.5*	*1.6*	*1.7*
2-6.1	Diameter	100.00 ± 0.50 mm		125.00 ± 0.50 mm
2-6.2	Primary Flat Length	32.5 ± 2.5 mm		42.5 ± 2.5 mm
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°		
2-6.4	Secondary Flat Length	18.0 ± 2.0 mm		27.5 ± 2.5 mm
2-6.5	Secondary Flat Location (see Figure 4) {111} *p*-type {100} *p*-type {111} *n*-type {100} *n*-type	No secondary flat 90° ± 5° clockwise from primary flat (θ = 180° ± 5°) 45° ± 5° clockwise from primary flat (θ = 225° ± 5°) 180° ± 5° from primary flat (θ = 90° ± 5°)		

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Property		*100 mm Wafers (t=525µm)*[#2]	*100 mm Wafers (t=625µm)*[#2]	*125 mm Wafers*[#2]
Previous SEMI Reference:		*SEMI M1.5*	*SEMI M1.6*	*SEMI M1.7*
Wafer Category:		*1.5*	*1.6*	*1.7*
2-6.6	Edge Profile Coordinate, C_y (T/3 Template, see Table ~~3~~ 10)	175 µm	208 µm	208 µm
2-6.7	Thickness, Center Point	525 ± 20 µm.	625 ± 20 µm	625 ± 20 µm
2-6.8	Total Thickness Variation, Max.	10 µm		
2-6.9	Bow, Max.	40 µm		
2-6.10	Warp, Max.	40 µm		

#4 Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.~~4~~1).

#5 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#6 For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

Table 5 Dimensional Characteristics of 150 mm Polished Single Crystal Silicon Wafers with Secondary Flat[#1]

Property		*150 mm Wafers*[#2]	
Previous SEMI Reference:		*SEMI M1.8*	
Wafer Category:		*1.8.1*	*1.8.2*
2-6.1	Diameter	150.00 ± 0.20 mm	
2-6.2	Primary Flat Length	57.5 ± 2.5 mm	
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°	
2-6.4	Secondary Flat Length	37.5 ± 2.5 mm	
2-6.5	Secondary Flat Location (see Figure 4) {111} *p*-type {100} *p*-type {111} *n*-type {100} *n*-type	 No secondary flat 90° ± 5° clockwise from primary flat (θ = 180° ± 5°) 45° ± 5° clockwise from primary flat (θ = 225° ± 5°) 135° ± 5° clockwise from primary flat (θ = 135° ± 5°)	
2-6.6	Edge Profile Coordinate, C_y	T/3 Template (see Table ~~3~~ 10) 225 µm	T/4 Template (see Table ~~3~~ 10) 169 µm
2-6.7	Thickness, Center Point	675 ± 20 µm	
2-6.8	Total Thickness Variation, Max.	10 µm	
2-6.9	Bow, Max.	60 µm	
2-6.10	Warp, Max.	60 µm	
2-5.7	Edge Surface Condition	Supplier-customer agreement[#4]	

#1 Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.~~4~~1).

#2 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the

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quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#3 For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

#4 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

Table 6 Dimensional Characteristics of 100 mm and 125 mm Polished Single Crystal Silicon Wafers without Secondary Flat[#1]

Property		*100 mm Wafers without secondary flat (t=525μm)[#2]*	*125 mm Wafers without secondary flat (t=625μm)[#2]*
Previous SEMI Reference:		*SEMI M1.11*	*SEMI M1.12*
Wafer Category:		*1.11*	*1.12*
2-6.1	Diameter	100.00 ± 0.20 mm.	125.00 ± 0.20 mm
2-6.2	Primary Flat Length	32.5 ± 2.5 mm	42.5 ± 2.5 mm
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°	
2-6.5	Secondary Flat Location	No secondary flat	
2-6.6	Edge Profile Coordinate, C_y (T/3 Template, see Table ~~3~~ 10)	175 μm	208 μm
2-6.7	Thickness, Center Point	525 ± 15 μm.	625 ± 15 μm
2-6.8	Total Thickness Variation, Max.	10 μm	
2-6.9	Bow, Max.	40 μm	
2-6.10	Warp, Max.	40 μm	

#1 Note that these specifications were originated in Japan. They are equivalent to the specifications for wafers of the same nominal diameter in JEITA EM-3602. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.~~4~~1).

#2 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#3 For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

Table 7 Dimensional Characteristics of 150 mm and 200 mm Polished Single Crystal Silicon Wafers without Secondary Flat[#1]

Property		*150 mm Wafers without secondary flat (t=625 μm)[#2]*		*200 mm Wafers flatted, without secondary flat[#2]*	
Previous SEMI Reference:		*SEMI M1.13*		*SEMI M1.10*	
Wafer Category:		*1.13.1*	*1.13.2*	*1.10.1*	*1.10.2*
2-6.1	Diameter	150.00 ± 0.20 mm		200.00 ± 0.20 mm	
2-6.2	Primary Flat Length	47.5 ± 2.5 mm		Not applicable	
	Flat Diameter	Not applicable		195.50 ± 0.20 mm	
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°			
2-6.5	Secondary Flat Location	No secondary flat			

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Property		*150 mm Wafers without secondary flat (t=625 µm)*[#2]		*200 mm Wafers flatted, without secondary flat*[#2]	
Previous SEMI Reference:		*SEMI M1.13*		*SEMI M1.10*	
Wafer Category:		*1.13.1*	*1.13.2*	*1.10.1*	*1.10.2*
2-6.6	Edge Profile Coordinate, C_y (see Table ~~3~~ 10)	T/3 Template 208 µm	T/4 Template 156 µm	T/3 Template 242 µm	T/4 Template 181 µm
2-6.7	Thickness, Center Point	625 ± 15 µm		725 ± 20 µm	
2-6.8	Total Thickness Variation, Max.	10 µm			
2-6.9	Bow, Max.	60 µm		65 µm	
2-6.10	Warp, Max.	60 µm		75 µm	
2-5.7	Edge Surface Condition	Not specified		Supplier-customer agreement[#4]	

#1 Note that these specifications were originated in Japan. They are equivalent to the specifications for wafers of the same nominal diameter in JEITA EM-3602. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.~~4~~1).

#2 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#3 For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

#4 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

Table 8 Dimensional Characteristics and Wafer ID Marking Requirements for Notched 200 mm and 300 mm Polished Single Crystal Silicon Wafers[#1]

Property		*200 mm Wafers (Notched)*[#2]			*300 mm Wafers (Notched)*[#2]	
Previous SEMI Reference:		*SEMI M1.9*			*SEMI M1.15*	
Wafer Category:		*1.9.1*	*1.9.2*	*1.9.3*	*1.15*	*1.15.1*
2-5.1	Wafer ID Marking	Supplier-customer agreement			SEMI T7 mark with optional A/N mark (see ¶ 6.5.1.4)	
2-5.7	Edge Surface Condition	Supplier-customer agreement[#3]			Polished[#3]	
2-6.1	Diameter	200.00 ± 0.20 mm			300.00 ± 0.20 mm	
2-6.2	Notch Dimensions (see Figure 5) Depth Angle	1.00 mm + 0.25 mm − 0.00 mm 90° + 5° − 1°				
2-6.3	Orientation of Notch Axis[#4]	<110> ± 1°				
2-6.5	Secondary Fiducial Location	No secondary fiducial				
2-6.6	Edge Profile[#5]	T/3 Template C_y = 242 µm	T/4 Template C_y = 181 µm	Edge profile parameters	T/4 Template C_y = 194 µm	Edge profile parameters
2-6.7	Thickness, Center Point	725 ± 20 µm			775 ± 20 µm	
2-6.8	Total Thickness Variation, Max.	10 µm			10 µm[#6]	
2-6.9	Bow, Max.	65 µm			Not specified	
2-6.10	Warp, Max.	75 µm			100 µm[#7]	
2-9.8	Back Surface Brightness (Gloss)	Not specified			0.80[#3,#8]	

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#1 Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see Note 5 following ¶ 6.6.4-1). The specification for 300 mm wafers is essentially equivalent to the specification for wafers of this diameter in JEITA EM-3602.

#2 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION**: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#3 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

#4 For 200 mm (111) wafers, the $[1\bar{1}0]$, $[01\bar{1}]$, and $[\bar{1}01]$ axes are the equivalent, allowable <110> axes. For (100) wafers, the allowable equivalent <110> axes are $[01\bar{1}]$, $[011]$, $[0\bar{1}1]$, and $[0\bar{1}\,\bar{1}]$.

#5 For edge profile coordinates C_y see Table ~~3~~ 10, and for the format of edge profile parameter specifications see Table ~~4~~ 11.

#6 Full wafer scan as described in SEMI MF1530.

#7 Warp corrected for gravitational effects. However, warp is not an adequate wafer shape specification for all applications.

#8 Gloss as measured in accordance with ASTM D523 or JIS Z 8741 with visible illumination at a 60° angle of incidence referenced to a mirror polished silicon wafer front surface. This metric may not describe the back surface finish adequately to establish detectability of small localized light scatterers (LLSs). If it is necessary to detect LLSs smaller than 0.25 µm LSE, another quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures shall be agreed upon between supplier and customer.

Table 9 Specified Requirements for Notched 450 mm Polished Single Crystal Silicon Wafers

Property		*450 mm Wafers*[#1, #2]	
Previous SEMI Reference:		*None*	
Wafer Category:		*1.16.1*	*1.16.2*
2-1.1	Growth Method	Supplier Option of Cz or MCz	
2-1.3	Conductivity Type	*p*	
2-1.4	Dopant	Boron	
2-1.6	FQA radius	223 mm	
2-1.8	Wafer Surface Orientation	(100) ± 0.5°	
2-5.1	Wafer ID Marking	SEMI T7	
2-5.7	Edge Surface Condition[#3]	Polished	
2-5.8	Back Surface Condition[#3]	Polished	
2-6.1	Diameter	450.00 ± 0.10 mm	
2-6.2	Notch Dimensions (see Figure 5) Depth Angle	 1.00 mm + 0.25 mm − 0.00 mm 90° + 5° − 1°	
2-6.3	Orientation of Notch Axis[#4]	<110> ± 1°	<010> ± 1°
2-6.5	Secondary Fiducial Location	No secondary fiducial	
2-6.6	Edge Profile Parameter Based Specification	Front edge width Front bevel angle Front shoulder radius Back shoulder radius Back bevel angle Back edge width	350 ± 50 µm 22.5º ± 3º 202.5 ± 42.5 µm 202.5 ± 42.5 µm 22.5º ± 3º 350 ± 50 µm
2-6.7	Thickness, Center Point	925 ± 20 µm	
2-6.8	Total Thickness Variation (GBIR)	≤3 µm	

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Property		*450 mm Wafers*[#1, #2]	
Previous SEMI Reference:		*None*	
Wafer Category:		*1.16.1*	*1.16.2*
2-6.9	Bow, Max	Supplier-customer agreement	
2-6.10	Warp[#5]	≤50 µm	
2-9.8	Back Surface Brightness (Gloss[#6])	0.80	

#1 For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. **CAUTION:** The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

#2 As time develops, these requirements may be altered; for example, *n*-type conductivity and phosphorus doping could be added.

#3 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

#4 For (100) wafers, the allowable equivalent <110> axes are [01$\bar{1}$], [011], [0$\bar{1}$1], and [0$\bar{1}\bar{1}$], and the equivalent <010> axes are [001], [0$\bar{1}$0], and [00$\bar{1}$].

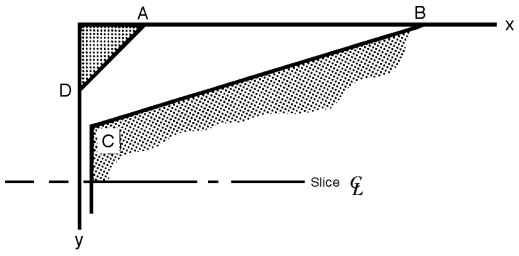
#5 Warp corrected for gravitational effects. However, warp is not an adequate wafer shape specification for all applications.

#6 Gloss as measured in accordance with ASTM D523 or JIS Z 8741 with visible illumination at a 60° angle of incidence referenced to a mirror polished silicon wafer front surface. This metric may not describe the back surface finish adequately to establish detectability of small localized light scatterers (LLSs). If it is necessary to detect LLSs smaller than 0.25 µm LSE, another quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures shall be agreed upon between supplier and customer.

~~6.6.2~~ 6.6.3 *Edge Profile* — The edge profile of edge-profiled wafers shall conform to either template-coordinate based or profile-parameter based specifications.

~~6.6.2.1~~ 6.6.3.1 *Template-Coordinate Based Specifications* — When specified according to a template, the edge profile of edge-profiled wafers shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches, if present).

~~6.6.2.1.1~~ 6.6.3.1.1 The SEMI Wafer Edge Profile Template is shown in Figure 6. There are two sets of dimensions for the template: T/3 and T/4, where T is the nominal thickness of the wafer (see Table~~s~~ ~~5~~ 3 through 8 ~~Table 10~~ for values of the nominal thickness for various wafer categories).



NOTE 1: The figure is not to scale.
NOTE 2: Only one-half of the template is shown; the wafer surface is aligned with the *x*-axis, and the outermost radial portion of the edge contour is aligned with the *y*-axis. The template in this figure is not intended for use in measuring wafer thickness.
NOTE 3: Constant radius profile with blended, tangential front and back surface intercepts is preferred for ease of manufacture and reduced particle and chip generation.
NOTE 4: The *x*- and *y*-axes in this template do not correspond with the *x*- and *y*-axes in the wafer coordinate system defined in SEMI M20.

Figure 6
SEMI Wafer Edge Profile Template

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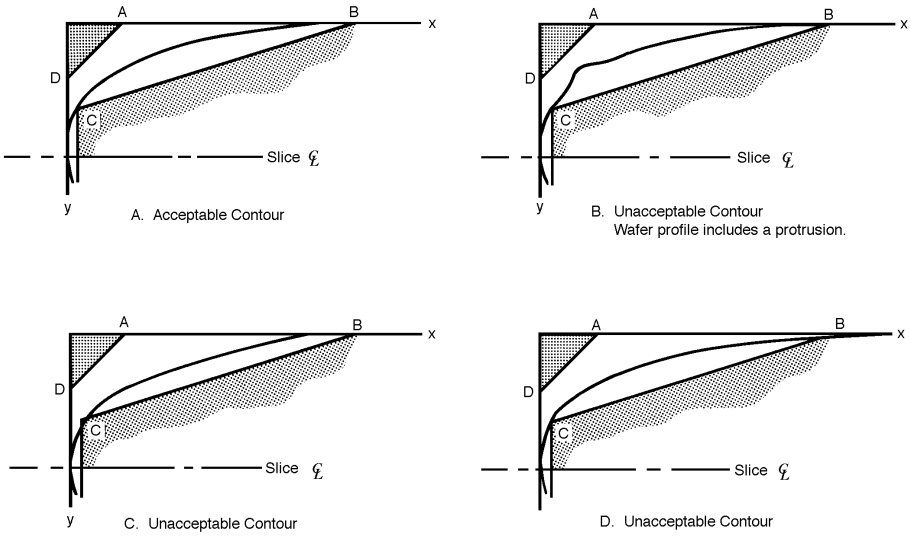
~~Table 3~~Table 10 Template-Coordinate Based Wafer Edge Profile Specifications (see Figure 6)

T/3 Wafer Edge Profile Template Coordinates				
Point	$x^{\#1}$		$y^{\#1}$	
A	0.0030 in.	76 µm	0.00 in.	0 µm
B	0.0200 in.	508 µm	0.00 in.	0 µm
C	0.0020 in.	50 µm	T/3[#2]	
D	0.00 in.	0 µm	0.0030 in.	76µm

T/4 Wafer Edge Profile Template Coordinates				
Point	$x^{\#1}$		$y^{\#1}$	
A	0.0047 in.	120 µm	0.00 in.	0 µm
B	0.0200 in.	508 µm	0.00 in.	0 µm
C	0.0040 in.	100 µm	T/4[#2]	
D	0.00 in.	0 µm	0.0020 in.	50 µm



#1 For referee purposes, U.S. Customary units are to be used for 2 inch and 3 inch diameter wafers SI units are to be used for all other wafers.

#2 For the value of this coordinate, see the specifications for the appropriate wafer category in Table ~~5~~ 3 through Table ~~10~~ 8.

Figure 7
Examples of Acceptable and Unacceptable Wafer Edge Profiles

~~6.6.2.1.2~~ 6.6.3.1.2 The coordinates for the two templates are given in Table ~~3~~ 10. Note that this coordinate system differs from that in SEMI M20 in that the origin is at the wafer edge instead of the wafer center and the *y*-axis is positive in the downward direction toward the wafer median plane instead of being in the plane of the wafer surface. If the nominal edge exclusion, *EE*, is 1 mm or greater, the edge profile will not extend into the FQA.

~~6.6.2.1.3~~ 6.6.3.1.3 When the wafer is aligned with the template so that the *x*-axis of the template is coincident with the wafer surface and the *y*-axis of the template is tangent with the outermost radial portion of the profile, the wafer edge profile must be contained within the clear region of the template (see Figure 7 for examples of acceptable and unacceptable edge profiles).

6.6.3.2 *Profile-Parameter Based Specifications* — The format of the specification is shown in Table ~~4~~ 11 together with a description of the parameters. Specification of the edge profile is done by completing this table using the specification value of each parameter together with its tolerance. These parameters are shown in the target profile of Figure ~~8~~ R2-1 along with the reference points that mark the transition from one segment to the next. § R2-2 provides instructions for constructing the target profile.

~~6.6.2.2~~ 6.6.3.2.1 Related Information 2 provides a procedure for drawing an envelope of the permitted parameter-based edge profiles that meet the specification. This envelope drawing may assist in understanding the limits of the parameter-based edge profile. However, unlike a template, not all profiles that fit within the envelope necessarily meet the specification.

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~~6.6.2.2.1~~ 6.6.3.2.2 Often front and back apex lengths and (less often) front and back apex angles are also specified. However, because the dimensions of the various segments of the edge profile in the vertical direction must add up to the specified thickness of the wafer, these dimensions are not independent of each other, but they are related by algebraic and trigonometric functions. The interdependency of these parameters is described as follows:

~~6.6.2.2.1.1~~ 6.6.3.2.2.1 In the *z*-direction, the distance from the origin to the end of the apex (reference point C_i) is simply b_i, the front or back apex length; the distance to the end of the shoulder segment (reference point B_i) is $r_i\cos\phi_i$; and the distance from the end of the shoulder segment to the surface is $[a_i - r_i(1-\sin\phi_i)\tan\phi_i]$, where here and elsewhere ~~in this Appendix~~ the subscript i represents f or b, as appropriate (see ¶ R2-1.2).

~~6.6.2.2.1.2 The sum of these three distances is simply half of the wafer thickness, $t/2$:~~

$$b_i + r_i\cos\phi_i + [a_i - r_i(1-\sin\phi_i)]\tan\phi_i = \frac{r_i(1-\sin\phi_i) + a_i\sin\phi_i + b_i\cos\phi_i}{\cos\phi_i} \quad (1)$$

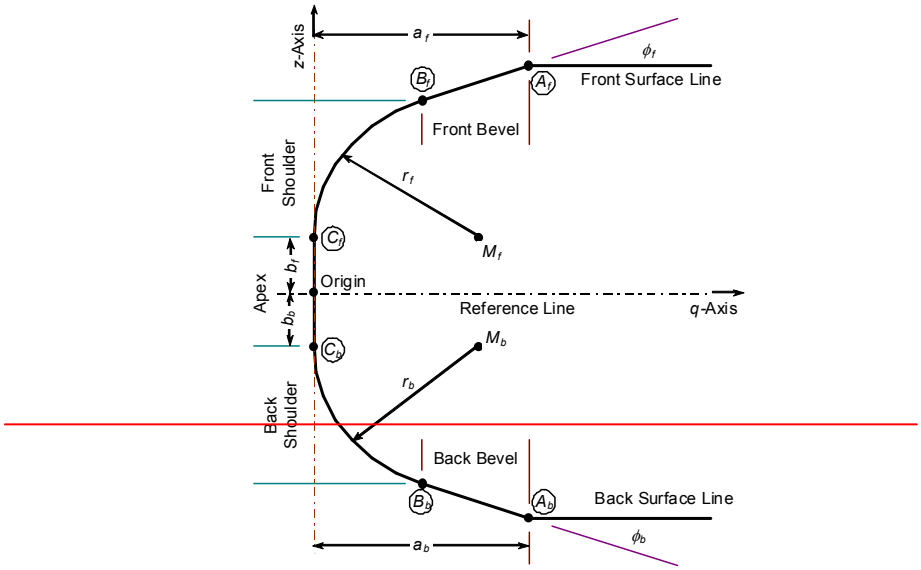
~~6.6.2.2.1.3 With the specification set given in Table 4, the apex lengths, b_i, are found from Equation 1 as follows:~~

$$b_i = \frac{t}{2} - r_i\cos\phi_i - [a_i - r_i(1-\sin\phi_i)]\tan\phi_i = \frac{1}{\cos\phi_i}\left[\frac{t\cos\phi_i}{2} - a_i\sin\phi_i - r_i(1-\sin\phi_i)\right] \quad (2)$$

~~Table 4~~Table 11 Parameters for Use with Profile-Parameter Based Edge Profile Specifications

Parameter Name	*Symbol*	*Value ± Tolerance*	*Unit*	*Explanation*
Front edge width	a_f		µm	Distance from the origin to the intersection of the front bevel and the front surface measured along an extension of the front surface.
Front bevel angle	ϕ_f		°	Angle between front surface and bevel, taken as positive into the wafer.
Front shoulder radius	r_f		µm	Radius of the arc of the front shoulder.
Back shoulder radius	r_b		µm	Radius of the arc of the back shoulder.
Back bevel angle	ϕ_b		°	Angle between back surface and bevel, taken as positive into the wafer.
Back edge width	a_b		µm	Distance from the origin to the intersection of the back bevel and the back surface measured along an extension of the back surface.
Thickness	t		µm	Specified value for the wafer on which the edge profile is being generated (see Tables 8 and 9, row 2-6.7).

~~Figure 8~~



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~~Schematic Drawing of a Model Edge Profile Illustrating the Terms, Symbols, and Reference Points Used to Describe the Profile~~

~~6.6.2.2.1.4~~ 6.6.3.2.2.2 This adjustment of the apex lengths within the *q*-*z* coordinate system with its origin on the median plane of the wafer is equivalent to the use of the surface-referenced *x*-*y* coordinate system of the traditional edge profile template of Figure 6 because it does not result in any change of the shape of the profile. On the other hand, if the apex length and two other parameters are specified, this is not the case because the shape of the profile can change when the parameters are varied within their allowed tolerances.

6.6.3.2.3 When specified according to a set of parameters, the edge profile of edge-profiled wafers shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches, if present). The measured values of the front and back edge width, bevel angle, and shoulder radius, as defined in Table 11 must fall within the specified tolerances. If desired, additional comparisons with the measured profile must fall within the range agreed upon between supplier and customer.

~~6.6.2.3.1 The measured values of the front and back edge width, bevel angle, and shoulder radius, as defined in Table 4 must fall within the specified tolerances. If desired, additional comparisons with the measured profile must fall within the range agreed upon between supplier and customer.~~

~~6.6.2.3.2 Alternatively, the measured profile must fall within a restricted-width, target-based template constructed in accordance with Appendix 3.~~

~~6.6.2.3~~ 6.6.3.3 Whether the edge profile is specified by template coordinates (see ¶ 6.3.3.1) or by a set of parameters (see ¶ 6.6.3.2), ~~or a specified template is specified,~~ no sharp points or protrusions are permitted anywhere on the wafer edge profile.

~~NOTE 4: Because no sharp points are permitted on the edge profile, the actual profile on the wafer has a transition between the edge and the wafer surface instead of the angular intersection shown in the model profile in Figure 8.~~

~~6.6.2.4~~ 6.6.3.4 Cosmetic attributes of the edge profile are not covered by either of these specifications. They shall be agreed upon between supplier and customer.

~~6.6.3~~ 6.6.4 *Shape* — The shape decision tree in Appendix ~~4~~ 3 fully describes the various shape parameters that can be specified.

~~6.6.3.1~~ 6.6.4.1 Warp is generally the shape parameter that is specified most often. Only wafers of category 1.1 (2 inch diameter) do not have a warp specification. Note that there are two forms of warp, one corrected for gravitational sag and the other not so corrected.

~~6.6.3.2~~ 6.6.4.2 If bow is specified, a sign may be included in the specification to denote convex (positive) or concave (negative) curvature of the median surface of the wafer with the front surface up. If no sign is included in the specification, bow may vary between −*a* and +*a*, where "*a*" is the specified maximum magnitude of bow.

~~6.6.3.3~~ 6.6.4.3 Sori is an attribute that may be specified with agreement between the supplier and customer in lieu of or in addition to bow and/or warp.

~~6.6.4~~ 6.6.5 *Flatness* — The wafers shall meet global and site flatness requirements as specified in the purchase order. Details of different flatness parameters are given in Appendix 1.

~~6.6.5~~ 6.6.6 *Nanotopography* — The wafers shall meet nanotopography requirements specified in the purchase order.

~~6.6.6~~ 6.6.7 *Near Edge Geometry* — The wafers shall meet near edge geometry requirements as specified in the purchase order. Note that the measurement method used is based on the particular near-edge geometry metric selected.

6.7 *Front Surface Chemistry*

6.7.1 If surface metal contamination levels are specified on the purchase order, the maximum area densities shall be designated in units of atoms/cm^2 for specific individual elements together with the measurement method by which the densities are to be determined. The wafers shall not contain more than the specified density of each metal.

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~~NOTE 5:~~ NOTE 6: An example of such a specification applicable to 1 µm geometries is given in Related Information ~~1~~ 3.

6.7.2 If surface organic contamination levels are specified on the purchase order, the maximum area densities shall be designated in units of ng/cm^2 for total surface organics density together with the method by which the density is to be determined. The wafers shall not contain more than the specified density of total surface organics.

~~Table 5~~Table 12 Polished Wafer Defect Limits

Item	*Characteristics*	*Maximum Defect Limit*	*AQL*[#1]	*Illumination Conditions*[#2]
FRONT SURFACE				
2-8.1	Scratches – Macro[#3]	None		Diffuse
2-8.2	Scratches – Micro[#3]	None		High Intensity
2-8.3	Pits[#3]	None	1% Cum.	High Intensity
2-8.4	Haze[#3]	None	1%	High Intensity
2-8.5	Localized Light Scatterers (LLS) (Contamination, Particulate)[#3] Maximum Number 2 in. Diameter Wafer 3 in. Diameter Wafer 100 mm Diameter Wafer 125 mm Diameter Wafer 150 mm Diameter Wafer	 4 6 10 10 15	1%	High Intensity
2-8.6	Contamination, Area[#3]	None	1%	High Intensity or Diffuse
2-8.7	Edge Chips and Indents[#4]	None	1% Cum. with Item 15[#5]	Diffuse
2-8.9	Cracks, Crow's Feet	None		Diffuse
2-8.10	Craters[#3]	None		Diffuse
2-8.11	Dimples[#3]	None		Diffuse
2-8.12	Grooves[#3]	None	1% Cum.	Diffuse
2-8.13	Mounds[#3]	None		Diffuse
2-8.14	Orange Peel[#3]	None		Diffuse
2-8.15	Saw Marks[#3]	None	1% Cum.	Diffuse
2-8.16	Resistivity Striations (Dopant Striation Rings)	None, except on low resistivity wafers[#6]		Diffuse
BACK SURFACE				
2-9.1	Edge Chips[#4]	None	1% Cum. with Item 6[#5]	Diffuse
2-9.3	Cracks, Crow's Feet	None		Diffuse
2-9.4	Contamination, Area	None	1% Cum.	Diffuse
2-9.5	Saw Marks[#7]	None	1% Cum.	Diffuse
ALL LISTED CHARACTERISTICS			Total 2.5%	

#1 Single, Normal, Level II Sampling Plan as defined in ANSI/ASQ Z1.4.

#2 See SEMI MF523 for definition of Illumination Conditions.

#3 The outer 0.062 inch (1.57 mm) annulus is excluded from these criteria.

#4 For wafers that are not mechanically edge-rounded, accept/reject criterion shall be agreed upon between supplier and customer.

#5 The cumulative AQL for both front surface and back surface of wafer is 1.0%.

#6 Striations may be visible on low resistivity wafers (<0.020 Ω·cm).

#7 For non-lapped wafers accept/reject criterion shall be agreed upon between supplier and customer.

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6.8 *Front and Back Surface Inspection Characteristics*

6.8.1 The wafers shall conform to the limits on observable (visually or otherwise) front and back surface characteristics as specified on the purchase order.

6.8.2 For wafers of diameter 150 mm or smaller for which visual inspection of surface defects is acceptable, the defect limits in Table 12 may be used as a guide for determining acceptable defect levels. Under these circumstances, minimal conditions or dimensions for surface features to be considered as defects are stated below. These limits shall be used for determining wafer acceptability; anomalies smaller than these limits shall not be considered defects.

6.8.2.1 *Item 2-8.1, Scratches, Macro* — Any anomaly conforming to the definition that has a length-to-width ratio greater than 5:1 and is visible under diffuse illumination as well as under high intensity illumination.

6.8.2.2 *Item 2-8.2, Scratches, Micro* — Any anomaly conforming to the definition that has a length-to-width ratio greater than 5:1 and is visible only under high intensity illumination.

6.8.2.3 *Item 2-8.3, Pits* — Any individually distinguishable nonremovable surface anomaly conforming to the definition that is visible when viewed under intense illumination.

6.8.2.4 *Item 2-8.4, Haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. Under some conditions, contamination may appear as haze.

6.8.2.5 *Item 2-8.5, Localized Light Scatterers (Particulate Contamination)* — Distinct particles or other surface anomalies resting on the surface that are revealed under collimated light as bright points.

6.8.2.6 *Items 2-8.6 and 2-9.4, Area Contamination* — Any foreign matter on the surface in localized areas that is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

6.8.2.7 *Items 2-8.7 and 2-9.1, Edge Chips and Indents* — Any edge anomaly including saw exit marks conforming to the definition that is greater than 0.25 mm (0.010 inch) in radial depth and peripheral length.

6.8.2.8 *Items 2-8.9a and 2-9.3a, Cracks* — Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 inch for 2 inch and 3 inch diameter wafers) in total length.

6.8.2.9 *Items 2-8.9b and 2-9.3b, Crow's Feet* — Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 in. for 2 inch and 3 inch diameter wafers) in total length.

6.8.2.10 *Item 2-8.10, Craters* — Any individually distinguishable surface anomaly conforming to the definition that is visible when viewed under diffused illumination.

6.8.2.11 *Item 2-8.11, Dimples* — Any smooth surface depression greater than 3 mm in diameter.

6.8.2.12 *Item 2-8.12, Grooves* — Any anomaly conforming to the definition that is greater than 0.13 mm (0.0005 inch for 2 inch and 3 inch diameter wafers) wide or 0.76 mm (0.030 inch for 2 inch and 3 inch diameter wafers) in length.

6.8.2.13 *Item 2-8.13, Mounds* — Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 inch for 2 inch and 3 inch diameter wafers) in maximum dimension.

6.8.2.14 *Item 2-8.14, Orange Peel* — Any visually detectable roughened surface conforming to the definition that is observable under diffused illumination.

6.8.2.15 *Items 2-8.15 and 2-9.5, Saw Marks* — Any anomaly conforming to the definition that is visible under diffuse illumination.

6.8.2.16 *Item 2-8.16, Resistivity Striations* (*Dopant Striation Rings*) — Any feature conforming to the definition that is detectable under diffused lighting conditions.

6.8.3 For other cases, acceptable surface defect levels shall be defined based on the use of surface scanning inspections systems (SSIS) for automated surface inspection. In this case, definitions of what surface anomalies constitute surface defects shall be agreed upon between supplier and customer.

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~~7 Basic Specification Without Optional Requirements~~

~~8~~ 7 Specifications for the 32, 22, and 16 nm Technology Generations

~~8.1~~ 7.1 Guides for the specification of 300 and 450 mm diameter prime polished wafers for the 32, 22, and 16 nm technology generations are given in Related Information 1. Note that the generation names are not universal and may vary by one or two nanometers from the listed value.

~~9~~ 8 Sampling

~~9.1~~ 8.1 Unless otherwise specified, ASTM E122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

~~10~~ 9 Test Methods

~~10.1~~ 9.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, or JIS standard test methods for the item as selected from Table 1 and specified in the purchase order.

~~NOTE 8:~~ NOTE 7: Although they are no longer supported nor supplied by DIN, DIN silicon standards are also listed in this section and may be used if available to the testing lab and agreed upon between supplier and customer. English translations of most of these standards are published in Volume 10.05 of the 1993 *Annual Book of ASTM Standards*, which may be available to some organizations. Titles of these standards are given in the Related Documents section.

~~10.2~~ 9.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

~~10.3~~ 9.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

~~10.4~~ 9.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

~~10.5~~ 9.5 Information about the various test methods listed in Table 1 is provided in Related Information ~~2~~ 4 together with information about some additional test methods no longer in wide use throughout the industry.

~~11~~ 10 Certification

~~11.1~~ 10.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

~~11.2~~ 10.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in § 9. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

~~12~~ 11 Product Labeling

~~12.1~~ 11.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in

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that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the customer.

~~12.2~~ 11.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶ 11.1 that is not included on the label shall be retained in the supplier's data base for at least one month after that particular lot has been accepted by the customer.

~~12.3~~ 11.3 Wafers of Categories 1.15 and 1.15.1 (300 mm in diameter) shall be shipped in packages labeled in accordance with SEMI M45.

~~13~~ 12 Packing and Shipping Container Labeling

~~13.1~~ 12.1 Special packing requirements shall be subject to agreement between the supplier and customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

~~13.2~~ 12.2 Wafers of Categories 1.15 and 1.15.1 (300 mm in diameter) shall be shipped in accordance with SEMI M45.

~~13.3~~ 12.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with CEA 556-C.

~~14~~ 13 Related Documents

~~14.1~~ 13.1 The following DIN standards are no longer supported or supplied by DIN but the can be used by organizations that have copies with agreement between supplier and customer.

DIN 50430 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals in Bars by Means of the Two-point-probe Direct Current Method

DIN 50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Four-Probe Array

DIN 50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

DIN 50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

DIN 50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

DIN 50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

DIN 50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

DIN 50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

DIN 50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

DIN 50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

DIN 50440/1 — Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples

DIN 50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

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DIN 50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

DIN 50441/3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

DIN 50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

DIN 50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

DIN 50444 — Conversion Between Resistivity and Dopant Density; Silicon

DIN 50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

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APPENDIX 1
FLATNESS DECISION TREE

NOTICE: The material in this Appendix is an official part of SEMI M1 and was approved by full letter ballot procedures on October 21, 1999 by the global Silicon Wafer Technical Committee.

A1-1 ~~Scope~~Introduction

A1-1.1 The increasing complexity of integrated circuits and the reduction in design rule dimensions place new demands on the characterization of wafer surface geometry. Various high resolution optical lithographic systems have very limited depth of field and use a variety of methods to hold the wafer, to establish the focal plane, and to position the wafer relative to the focal plane during exposure. These varying focusing and location methods differ enough to make a single, simple flatness criterion (such as global TIR) ineffective in predicting successful or unsuccessful lithography in all cases.

A1-1.2 To clarify the requirements for wafer flatness characterization for the various classes of lithographic equipment, the decision tree depicted in Figure A1-1 has been developed. This tree gives an orderly procedure for selecting the various parameters that must be specified if wafer flatness is specified.

A1-1.3 In this tree, it is assumed that the focal point is the site center for all parameters, except for SFQD, SFQR, SFSD, and SFSR, where the focal plane is identical to the reference plane. Most flatness characterization systems employ this convention. However, a number of photolithographic aligners use slightly different conventions for determining the focal plane. Currently, the difference between the centerpoint and other focusing conventions has not been quantified, but it is presumed to be insignificant for material characterization purposes.

A1-1.3.1 For sites to be included in the measurement, the site center must lie within the FQA. For subsites (see Figure A1-2) to be included in the measurement, the subsite center must lie within a site whose center is within the FQA and some of the subsite must lie within the FQA (see Figure A1-3).

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A1-2 Use of the Flatness Decision Tree

A1-2.1 In the decision tree, there are decision blocks, shown as diamonds, whose use requires some knowledge of the lithographic tool to be used. The rectangular blocks require information to be furnished; this information is dependent on the device layout and the manufacturing procedures to be employed (such as dedicated or mixed aligner use).

A1-2.2 *Step 1* — Select the FQA: Decide on and specify the nominal edge exclusion, *EE*, which defines the FQA (see Figure 1).

A1-2.3 *Step 2* — Choose the Measurement Method: Choose global flatness (G) if the lithographic tool uses a single, global exposure of the wafer, or choose site flatness (S) if the lithographic tool steps across the wafer, exposing only a portion of the wafer at a time.

A1-2.3.1 If global flatness is chosen, proceed to Step 3. If site flatness is chosen, it is also necessary to specify site size (related to exposure area dimensions) and site array (including (a) number of sites, (b) location of sites relative to the center of the FQA and to each other, as in an offset or bricklaying pattern, and (c) whether or not partial sites are to be excluded).

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A1-2.4 *Step 3* — Choose the Reference Surface: Choose front surface (F) or back surface (B), depending on whether the lithographic tool is referenced to the front or back surface.

A1-2.5 *Step 4* — Choose the Reference Plane and Area:

A1-2.5.1 For global flatness measurements, a global reference plane is appropriate. If the lithographic tool is referenced to the back surface, an ideal plane (I) defined by the chuck which holds the wafer is appropriate. If the lithographic tool is referenced to the front surface, either a 3-point plane (3) defined by three points equally spaced about the edge of the front surface of the wafer or a plane defined by the least squares fit to the front surface (L) may be appropriate. The 3-point plane is appropriate if the lithographic tool holds the wafer in this fashion and does not allow interactive gimbaling of the wafer, while the least squares plane is appropriate if the lithographic tool allows interactive gimbaling of the wafer.

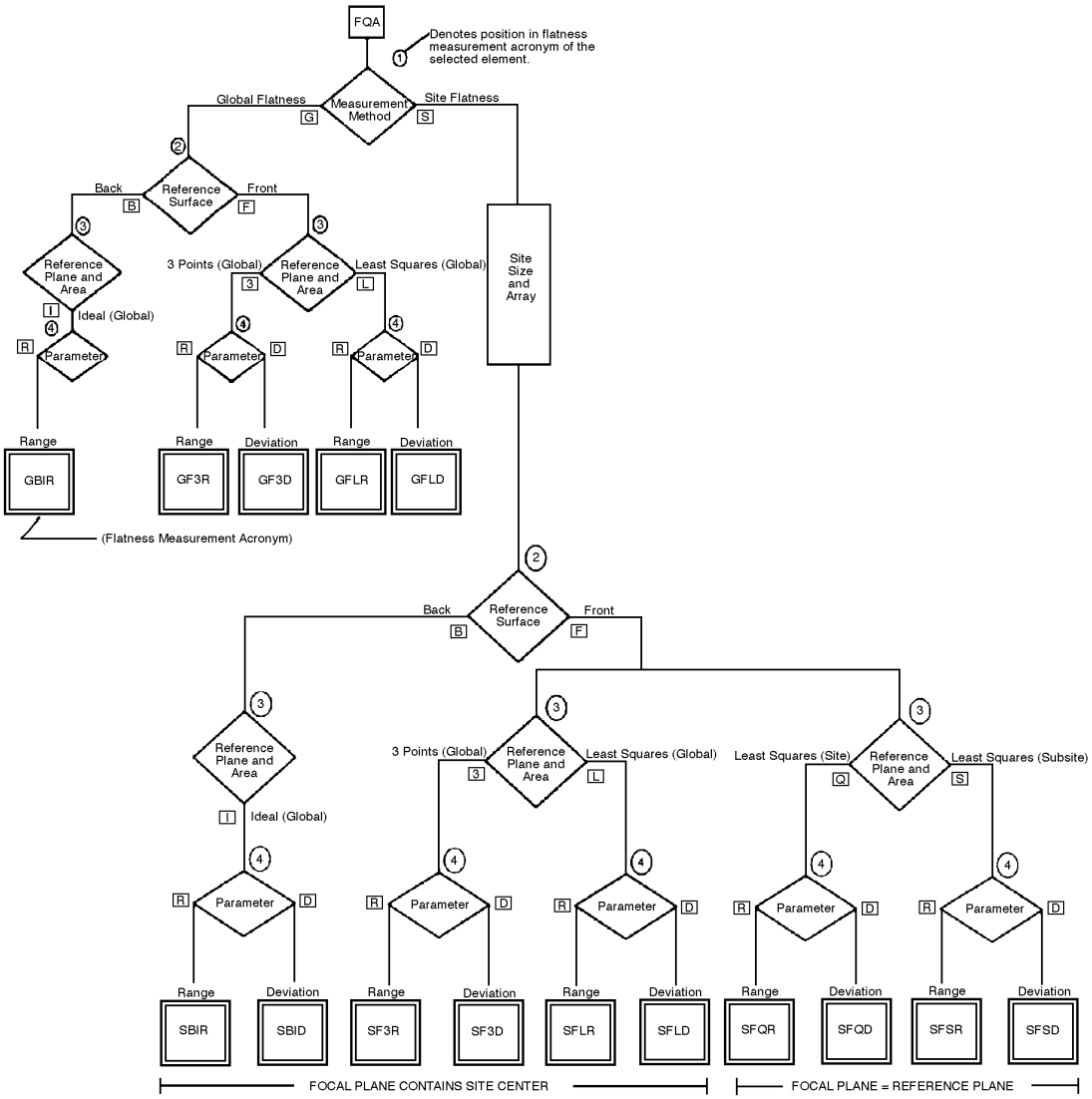

Figure A1-1
Flatness Decision Tree

A1-2.5.2 For site flatness measurements, any of the above three planes [(1), (3), or (L)] may be suitable or, if the wafer is regimballed once at each site, a site least squares reference plane (Q) may be appropriate or, if the wafer is regimballed more than once at each site, a subsite least squares reference plane (S) may be appropriate.

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A1-2.6 *Step 5* — Choose the Measurement Parameter: Choose either TIR, also known as range (R), or FPD, also known as deviation (D). In the case of site measurements, it is possible to specify the maximum value of (R) or (D) or the percentage of the sites (or FQA) which have an (R) or (D) less than some specified value.

A1-2.7 The codes in parentheses in Steps 2 through 5 may be used to form a code which uniquely defines the measurement technique as follows:

- Position 1: Measurement Method (G) or (S),
- Position 2: Reference Surface (F) or (B),
- Position 3: Reference Plane and Area (I), (3), (L), (Q), or (S), and
- Position 4: Measurement Parameter (R) or (D).

A1-2.7.1 Stating this code, the numerical values for the FQA parameters (and, if required, information on site size and array), and the numerical limit for the measurement parameter provides enough information to describe the measurement and provide numerical limits.

A1-3 Future Developments

A1-3.1 As noted above, there may be specific systems which are not exactly described by one of the branch ends on this decision tree. This tree is an approximation of the more complete one which would describe all existing and possible lithographic technologies.

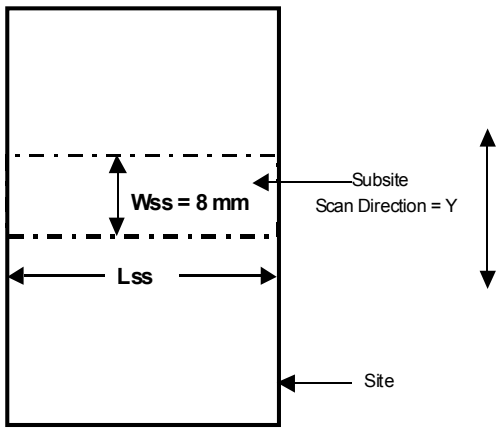

Figure A1-2
Scanner Site and Subsite Flatness Elements

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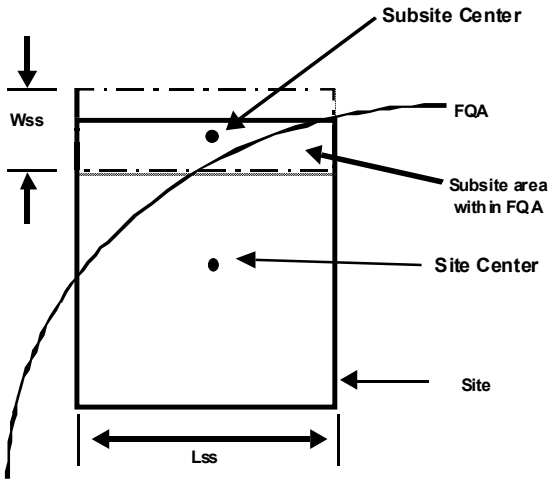

Figure A1-3
Subsite Center near Boundaries of Site and FQA

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APPENDIX 2
RoHS REQUIREMENTS

NOTICE: The material in this Appendix is an official part of SEMI M1 and was approved by full letter ballot procedures on January 18, 2007 by the global Silicon Wafer Technical Committee.

A2-1 ~~Scope~~Introduction

A2-1.1 At present, the only publically available directive on this topic known to the developers of this Standard is that of the European Community. As additional directives become publically available, they will be added to this Standard.

A2-2 European Community Directive

~~A2-1.2~~ A2-2.1 The European Parliament and Council issued directive 2002/95/EC on January 27, 2003. The objective of this directive is "…to approximate the laws of the Member States on the restriction of the use of hazardous materials in electric and electronic equipment…" for reasons of health protection and environmentally sound recovery of disposal of waste electrical and electronic equipment. The following are included among the categories of such equipment:

- small and large household equipment, consumer equipment
- IT and telecommunication equipment
- lighting equipment, electrical and electronic tools
- toys, leisure and sports equipment
- automatic dispensers

~~A2-1.2~~ A2-2.2 Maximum concentrations tolerated in homogeneous materials were defined in an amendment to Directive 2002/95/EC on September 23, 2004:[9]

- 1000 ppmw for Pb, Hg, hexavalent Cr, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE)
- 100 ppmw for Cd

~~A2-1.3~~ A2-2.3 This directive became European law on July 1, 2006, and some European member states have already corresponding laws in place.

~~**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.~~

~~**A2-2**~~ A2-2.4 *Referenced Standards and Documents*

~~A2-2.1~~ A2-2.4.1 CEA Standard[10]

CEA JIG-101 — Material Composition Declaration for Electrotechnical Products

[9] Council decision amending Directive 2002/95/EC of the European Parliament and of the Council for the purposes of establishing the maximum concentration values for certain hazardous substances in electrical and electronic equipment, COM(2004)606 final. Available for downloading from the following URL: http://europa.eu.int/eur-lex/en/com/pdf/2004/com2004_0606en01.pdf.

[10] Consumer Electronics Association, 1919 S. Eads St., Arlington, VA 22202, USA. Telephone: 703.907.7634; Fax: 703.907.7693; http://www.ce.org

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~~A2-2.2~~ A2-2.4.2 CEN Standard[11]

CEN EN 1483 — Water Quality – Determination of Mercury – Method Using Atomic Absorption Spectrometry

~~A2-2.3~~ A2-2.4.3 ISO Standards[12]

ISO 11885 — Water Quality – Determination of Selected Elements by Inductively Coupled Plasma Optical Emission Spectroscopy (ICP-OES)

ISO 10304-3 — Water Quality – Determination of Dissolved Anions by Liquid Chromatography of Ions – Part 3: Determination of Chromate, Iodide, Sulfite, Thiocyanate and Thiosulfate

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

~~**A2-3**~~ A2-2.5 *Requirements and Test Methods*

~~A2-3.1~~ A2-2.5.1 Currently tolerated maximum concentrations of hazardous materials in homogeneous materials are listed in Table A2-1. The flame retardants, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), are not expected to occur in semiconductor grade Si or on Si wafers. Their tolerated maximum concentrations are listed in the table for the sake of completeness. The test methods listed in Table A2-1 may be applied to silicon wafers only after appropriate extraction of metals with acid or alkaline solutions. Alternative test methods may be used provided that (1) they determine the total content in the wafer of the hazardous material being tested for and (2) the results obtained are equivalent to those obtained by the listed methods.

Table A2-1 Tolerated Maximum Concentrations of Hazardous Materials in or on Silicon Wafers

Hazardous material	*Maximum Concentration*[#1]	*Maximum Concentration*	*Maximum Density*	*Test Method*[#2]
Cr(VI)	1000 ppmw	540 ppma	27×10^{18} atoms/cm^3	ISO 10304-3
Cd	100 ppmw	25 ppma	1.25×10^{18} atoms/cm^3	ISO 11885
Hg	1000 ppmw	140 ppma	7×10^{18} atoms/cm^3	CEN EN 1483
Pb	1000 ppmw	136 ppma	6.8×10^{18} atoms/cm^3	ISO 11885
Polybrominated Biphenyls (PBB)	1000 ppmw	29–120 ppm molecules[#3]	$1.5\text{-}6 \times 10^{18}$ molecules/cm^3[#4]	X-ray fluorescence analysis of Br
Polybrominated Diphenyl Ethers (PBDE)	1000 ppmw	29-120 ppm molecules[#3]	$1.5\text{-}6 \times 10^{18}$ molecules/cm^3 [#4]	X-ray fluorescence analysis of Br

#1 As required by Directive 2002/95/EC, see also CEA JIG-101.

#2 To be applied with appropriate acid or alkaline extraction method.

#3 Value is rounded and depends on number of Br atoms per molecule PBB or PBDE.

#4 Value is rounded and depends on number of Br atoms per molecule PBB or PBDE.

~~**A2-4**~~ A2-2.6 Testing and Certification

~~A2-4.1~~ A2-2.6.1 The provisions of § 9 and § 10 relating to testing and certification shall apply to the testing listed in Table A2-1.

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[12] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; http://www.iso.ch

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~~APPENDIX 3~~
~~TARGET-BASED TEMPLATE FOR PARAMETER-SPECIFIED EDGE PROFILES~~

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~~APPENDIX 4~~APPENDIX 3
SHAPE DECISION TREE

NOTICE: The material in this Appendix is an official part of SEMI M1 and was approved by full letter ballot procedures on October 21, 1999 by the global Silicon Wafer Technical Committee.

~~A4-1~~ A3-1 ~~Scope~~Introduction

~~A4-1.1~~ A3-1.1 In modern wafer fabrication processes, wafer surface geometry in the unclamped state can be a sensitive indicator of process effects. Larger wafer diameters and increasing complexity of processes and circuits have increased the need for accurate, standardized measurement of unclamped wafer geometry. The quantities that have historically been used, Bow and Back Surface Referenced Warp, may be inadequate to describe and quantify the geometries of interest in advanced processes. Additional surface geometry quantities, such as Sori and Median Surface Referenced Warp, have been introduced into standards.

~~A4-1.2~~ A3-1.2 In addition, there is considerable confusion as to the precise meaning of these quantities, even though they are defined in the applicable SEMI test methods.

~~A4-1.3~~ A3-1.3 The Shape Decision Tree was developed to provide an orderly method of identifying each of the variables involved in the quantities used to quantify unclamped wafer surface geometry. As such, the tree provides a concise and precise description of each shape quantity. A branch of the tree consists of a selection of one of the choices for each variable. The variables and the choices for each are listed in Table ~~A4~~A3-1.

~~A4-1.4~~ A3-1.4 Four branches of the tree, representing quantities for which measurement methods have been standardized by SEMI, are depicted in Figure ~~A4~~A3-1. There are many other branches of the tree, not all of which may represent practical combinations of variables.

~~**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.~~

~~A4-2~~ A3-2 Use of the Shape Decision Tree

~~A4-2.1~~ A3-2.1 *Step 1* — Select the FQA: Decide on and specify the nominal edge exclusion, *EE*, which defines the FQA (see Figure A3-1).

~~A4-2.2~~ A3-2.2 *Step 2* — Select the measurement method: global (over the entire FQA) or local (over a site).

NOTE 1: At present, all shape quantities in common use are global measurements. The significance and use of local shape quantities have yet to be defined.

~~A4-2.3~~ A3-2.3 *Step 3* — Select the reference surface: front, median, or back, to be used to establish the reference plane.

~~A4-2.4~~ A3-2.4 *Step 4* — Select the kind of reference plane: least-squares or 3-point.

NOTE 2: A measurement made with a least-squares reference plane is less affected by small changes in wafer position within the measurement apparatus than is a measurement made with a 3-point reference plane.

~~A4-2.5~~ A3-2.5 *Step 5* — Determine whether the effects of gravitational sag on the wafer are accounted for (yes) or not (no).

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NOTE 3: Gravitational effects may be accounted for by inverting the wafer during the measurement, by placing the wafer in a vertical or nearly vertical position during the measurement, or mathematically.

~~A4-2.6~~ A3-2.6 *Step 6* — Select the measurement surface: front, median, or back, for which the deviations are to be measured.

~~A4-2.7~~ A3-2.7 *Step 7* — Select the measurement pattern: full scan (a regular array of measurement points over the entire measurement area), partial scan (a specified pattern of measurement points covering only a portion of the measurement area), or centerpoint (measurement at the center of the wafer only).

~~A4-2.8~~ A3-2.8 *Step 8* — Select the parameter to be determined: range (TIR) or maximum RPD.

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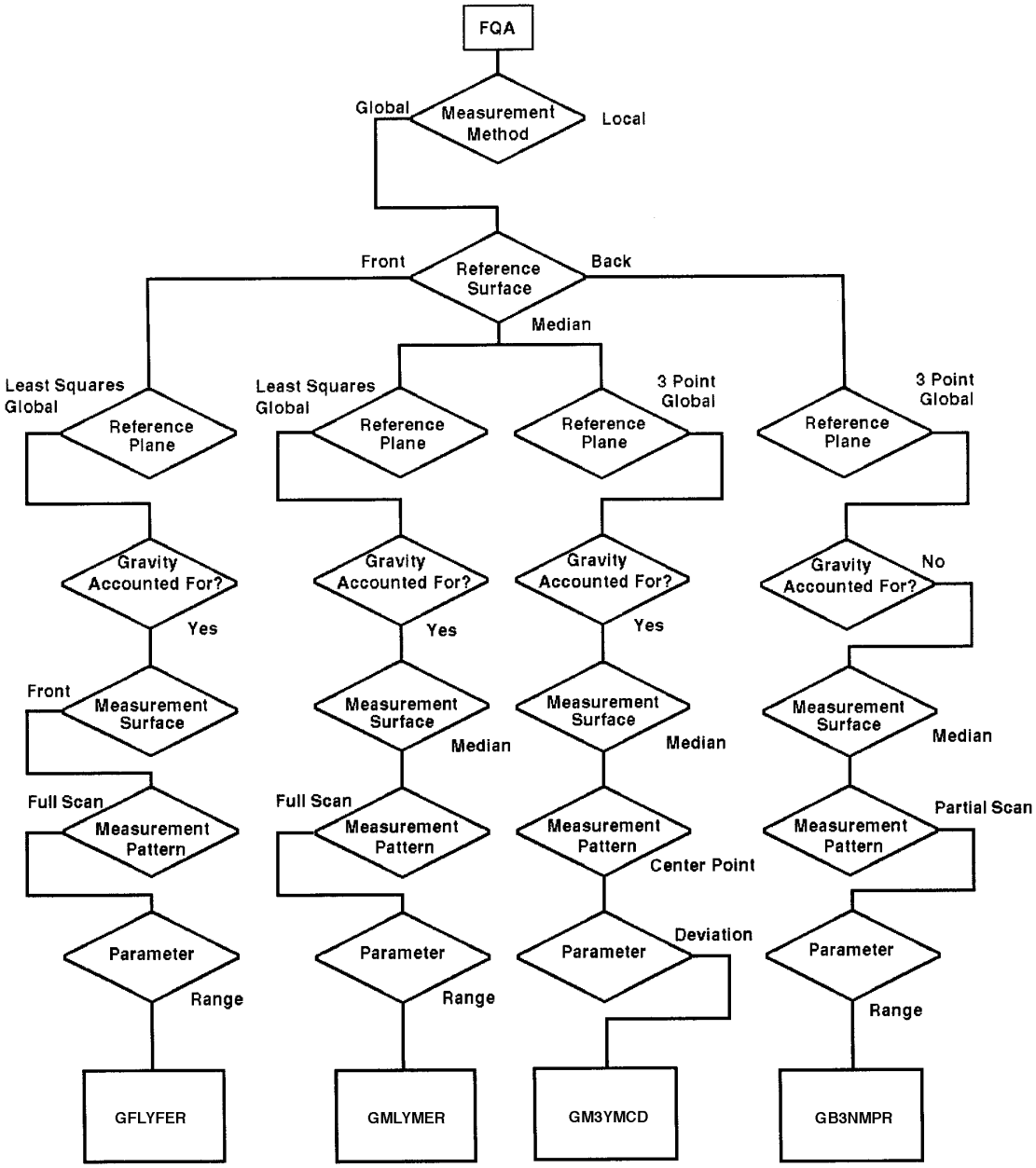

Figure A3-1
Four Branches of the Shape Decision Tree

~~A4-2.9~~ A3-2.9 *Step 9* — Compare the branch thus obtained with the branches in Figure ~~A4~~A3-1. If the branch obtained matches one of the branches illustrated in Figure ~~A4~~A3-1, the resulting quantity is given by the code shown in the box at the bottom of the branch. Standard test methods have been adopted for measurement of each of these quantities. If the branch obtained does not match any of the branches illustrated in Figure ~~A4~~A3-1, the quantity obtained has not been given a standardized term, nor has a standard test method been adopted for its measurement.

~~A4-2.9.1~~ A3-2.9.1 These codes, which uniquely describe the various branches, are formed from the codes in Table ~~A4~~A3-1. Stating this code together with the numerical value for the FQA nominal edge exclusion provides enough information to describe the shape parameter and to establish numerical limits for it.

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~~A4-2.9.2~~ A3-2.9.2 Table ~~A4~~A3-2 summarizes the shape parameters for which SEMI has standardized test methods. This table lists the code, the term in common use for the parameter, the SEMI Test Method, and the expanded form of the code.

Table A3-1 Variables in Shape Quantities

Variable	*Options*	*Code*
Measurement Method	Global	G
	Local (Site)	S
Reference Surface	Front	F
	Median	M
	Back	B
Reference Plane	Least-square	L
	3-point	3
Corrected for Gravitational Sag	Yes	Y
	No	N
Measurement Surface	Front	F
	Median	M
	Back	B
Measurement Pattern	Full Scan (Entire)	E
	Partial Scan	P
	Centerpoint	C
Parameter	Range (TIR)	R
	Maximum RPD	D

Table A3-2 Shape Code Summary

Code	*Term*	*Test Method*	*Expanded Form of Code*
GFLYFER	sori	SEMI MF1451	Global, Front-surface Least-squares reference plane, Yes (corrected for gravitational sag), Front-surface measurement, Entire surface scanned, Range
GMLYMER	warp	SEMI MF1390	Global, Median-surface Least-squares reference plane, Yes (corrected for gravitational sag), Median-surface measurement, Entire surface scanned, Range
GM3YMCD	bow	SEMI MF534	Global, Median-surface 3-point plane, Yes (corrected for gravitational sag), Median-surface measurement at Center point, Deviation
GB3NMPR	warp	SEMI MF657	Global, Back-surface 3-point reference plane, No (not corrected for gravitational sag), Median-surface measurement, Partial surface scanned, Range

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RELATED INFORMATION 1

SPECIFICATION GUIDES FOR ADVANCED TECHNOLOGY GENERATIONS

NOTICE: This Related Information is not an official part of SEMI M1 and was derived from the work of the global Silicon Wafer Technical Committee. This Related Information was approved for publication by full letter ballot procedures on June 28, 2012.

R1-1 Introduction

R1-1.1 Specification Guides for polished prime wafers used in advanced technology are useful to facilitate rapid implementation and standardization of wafers in new technology generations. Although the impetus for this development was the transition to 450 mm diameter wafers, the guides are not diameter specific.

R1-2 Specification Guides for 32, 22, and 16 nm Technology Generations

R1-2.1 Table R1-1 provides specification guides for 300 and 450 mm diameter prime polished wafers to be used in the 32, 22, and 16 nm technology generations

~~NOTE 4:~~ NOTE 1: Technology generations may cover a region a few nanometers from the listed value.

Table R1-1 Guide for the Specification of 300 and 450 mm Diameter Silicon Wafers for the 32, 22, and 16 nm Technology Generations

Technology Generation[#1]		*32 nm*	*22 nm*	*16 nm*	*Measurement Method*
2-1 **GENERAL CHARACTERISTICS**					
2-1.1	Growth Method	Cz or MCz			
2-1.3	Crystal Orientation	(100)			SEMI MF26 (x-ray)
2-1.4	Conductivity Type	*p* or *n* (Customer Specified)			SEMI MF42
2-1.5	Dopant	B (for *p*-type) or P (for *n*-type)			SEMI MF1389
2-1.6	FQA radius 300 mm wafers 450 mm wafers	 148 mm 223 mm			
2-1.8	Wafer surface declination in respect to crystal orientation	On-orientation $0.00^0 \pm 1.00^0$			SEMI MF26 (x-ray)
2-2 **ELECTRICAL CHARACTERISTICS**					
2-2.1	Resistivity	Customer Specified			SEMI MF673
2-2.2	Radial Resistivity Variation[#2]	<10%			SEMI MF81
2-3 **CHEMICAL CHARACTERISTICS**					
2-3.1	Oxygen Concentration	Customer Specified			SEMI MF1188, SEMI MF1366
2-3.2	Radial Oxygen Variation[#3]	≤10%			SEMI MF951
2-3.3	Carbon Concentration	Customer Specified			SEMI MF1391
2-4 **STRUCTURAL CHARACTERISTICS**					
2-4.1	Dislocation Etch Pit Density	$\leq 10/cm^2$			SEMI MF1809
2-4.2	Slip	None			SEMI MF1809
2-4.4	Twin Boundary	None			SEMI MF1809
2-4.5	Swirl	None			SEMI MF1809

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Technology Generation[#1]		*32 nm*	*22 nm*	*16 nm*	*Measurement Method*
2-5 **WAFER PREPARATION CHARACTERISTICS**					
2-5.1	Wafer ID Marking	SEMI T7			SEMI T7
2-5.7	Edge surface conditions	Polished[#4]			
2-5.8	Back surface condition	Polished[#4]			
2-6 **DIMENSIONAL CHARACTERISTICS**					
2-6.1	Diameter 300 mm wafers 450 mm wafers	300 ± 0.2 mm 450 ± 0.1 mm			SEMI M1, SEMI MF2074
2-6.2	Notch dimensions Depth Angle	1.00 + 0.25 − 0.00 mm 90° + 5° − 1°			SEMI MF1152
2-6.3	Orientation of Notch axis	<110> ± 1°			
2-6.6	Edge profile 300 mm wafers 450 mm wafers	Customer Specified (T/4 Template or Parameter) Customer Specified (Parameter)			SEMI M1, SEMI M73 SEMI M73
2-6.7	Thickness, center point 300 mm wafers 450 mm wafers	775 ± 20 µm 925 ± 20 µm			SEMI MF533
2-6.8	GBIR, less than	3 µm			SEMI MF1530
2-6.10	Warp[#5]	≤50 µm			
2-6.13	Flatness/SFQR [#6] (26 mm × 8 mm site size)	32 nm	22 nm	16 nm	SEMI MF1530
2-6.14	Nanotopography [#7]2 × 2 mm	8 nm	6 nm	5 nm	SEMI M78
2-6.15	Near Edge Geometry	Customer Specified			SEMI M67 (ESFQR), SEMI M68 (ZDD)
2-7 **FRONT SURFACE CHEMISTRY**					
2-7.1.1	Sodium	$\leq 1 \times 10^{10}$ cm^{-2}			SEMI MF1617, SEMI E45 ISO 17331
2-7.1.2	Aluminum	$\leq 1 \times 10^{10}$ cm^{-2}			SEMI MF1617, SEMI E45 ISO 17331
2-7.1.3	Potassium	$\leq 1 \times 10^{10}$ per cm^2			SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.4	Chromium	$\leq 1 \times 10^{10}$ cm^{-2}			SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.5	Iron	$\leq 1 \times 10^{10}$ cm^{-2}		$\leq 5 \times 10^{9}$ cm^{-2}	SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.6	Nickel	$\leq 1 \times 10^{10}$ cm^{-2}		$\leq 5 \times 10^{9}$ cm^{-2}	SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.7	Copper	$\leq 1 \times 10^{10}$ cm^{-2}		$\leq 5 \times 10^{9}$ cm^{-2}	SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.8	Zinc	$\leq 1 \times 10^{10}$ per cm^2			SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-7.1.9	Calcium	$\leq 1 \times 10^{10}$ per cm^2			SEMI M33, SEMI MF1617 SEMI E45, ISO 17331
2-8 **FRONT SURFACE INSPECTION CHARACTERISTICS**					
2-8.1	Scratches – Macro	None			SEMI MF523
2-8.2	Scratches – Micro	None			SEMI MF523
2-8.3	Pits (COP)	Customer Specified			SEMI MF523

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Technology Generation[#1]		*32 nm*	*22 nm*	*16 nm*	*Measurement Method*
2-8.4	Haze	Customer Specified			SEMI MF523
2-8.5	Localized Light Scatterers				SEMI M53, SEMI M58
	- size	≥45 nm	≥32 nm	≥32 nm	
	- density	≤0.19 cm^{-2}	≤0.19 cm^{-2}	≤0.18 cm^{-2}	
2-8.6	Edge Chips	None			SEMI MF523
2-8.11	Dimples	None			SEMI MF523
2-8.14	Orange Peel	None			SEMI MF523
2-9 **BACK SURFACE INSPECTION CHARACTERISTICS**					
2-9.1	Edge Chips	None			SEMI MF523
2-9.2	Edge Cracks	None			SEMI MF523
2-9.4	Contamination/Area	None			SEMI MF523
2-9.6	Stains	None			SEMI MF523
2-9.9	Scratches – Macro	None			SEMI MF523
2-9.10	Scratches – Micro	None			SEMI MF523
2-9.11	Localized Light Scatterers	Customer Specified			SEMI M53, SEMI M58

#1 The nominal Technology Generation (node) numbers given in this document and in other Silicon Wafer Committee Standards use a scaling rule of 1 / √2 (~0.7) per generation. This is similar to the 2010 Litho Focus DRAM ½ pitch table in the ITRS. This may differ from latest industry or other ITRS practice by a few nanometers.

#2 For 300 mm wafers center to 6 mm from the edge; for 450 mm wafers measured between Center Point and a point on a radius 219 mm from the Center Point.

#3 For 300 mm wafers center to 10 mm from the edge; for 450 mm wafers measured between Center Point and a point on a radius 215 mm from the Center Point.

#4 Implies a surface condition and not a particular processing technique

#5 Warp corrected for gravitational effects. However, warp is not an adequate wafer shape specification for all applications.

#6 The SFQR values are maximum values including partial sites and follow ITRS guidance where SFQR equals nominal node value for DRAM ½ pitch.. These values are considered challenging. SFQR specifications may be agreed upon between supplier and customer.

#7 The Nanotopography values follow ITRS using node values for DRAM ½ pitch.. These values are considered challenging. Nanotopography specifications may be agreed upon between supplier and customer.

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RELATED INFORMATION 2
PROFILE-PARAMETER BASED EDGE PROFILE ENVELOPES

NOTICE: This related information is not an official part of SEMI M1 and was derived from the work of the global Silicon Materials Committee. This related information was approved for publication by full letter ballot on [date tbd]

R2-1 Introduction

R2-1.1 The target edge profile of a profile-parameter based wafer edge profile specification is based on the value of the parameters listed in Table 11. Typical parameter values and their tolerances for 300 and 450 mm diameter wafers are given in Table R2-1.

Table R2-1 Typical Parameter Values and Their Tolerances

Parameter Name	*Symbol*	*Target Value of Parameter*	*Tolerance of Parameter*
Front edge width	a_f	350 µm	±50 µm
Front bevel angle	ϕ_f	22.5°	±3°
Front shoulder radius	r_f	202.5 µm	±42.5 µm
Back shoulder radius	r_b	202.5 µm	±42.5 µm
Back bevel angle	ϕ_b	22.5°	±3°
Back edge width	a_b	350 µm	±50 µm

R2-1.2 In accordance with the discussion in § 6.6.2.2.1, resulting in equation (2), the front apex length, b_f, is given by:

$$b_f = \frac{1}{\cos\phi_f}\left[\frac{t\cos\phi_f}{2} - a_f\sin\phi_f - r_f\left(1-\sin\phi_f\right)\right] \quad \text{(R2-1)}$$

and the back apex length, b_b, is given by:

$$b_b = \frac{1}{\cos\phi_b}\left[\frac{t\cos\phi_b}{2} - a_b\sin\phi_b - r_b\left(1-\sin\phi_b\right)\right]. \quad \text{(R2-2)}$$

R2-1.3 Although the parameter values in Table R2-1 are the same for both 300 mm and 450 mm diameter wafers, the standardized thicknesses differ. Consequently, the magnitudes of the front and back apex lengths also differ. The apex lengths for target profiles are given in Table R2-1. Note that the tolerance given is only for the thickness variation and is not that which results from changing the profile parameters from their target values.

Table R2-2 Apex Lengths for 300 and 450 mm Diameter Wafer Target Profiles

Parameter Name	*Symbol*		
Nominal wafer diameter	d	300 mm	450 mm
Standard thickness	t	775 ± 20 µm	925 ± 20 µm
Front apex length	b_f	107.22 ± 10 µm	182.22 ± 10 µm
Back apex length	b_b	107.22 ± 10 µm	182.22 ± 10 µm

R2-1.4 Note that, as indicated in ¶ 6.6.2.2.1.4, this adjustment of the apex lengths within the q-z coordinate system with its origin on the median plane of the wafer is equivalent to the use of the surface-referenced x-y coordinate system of the traditional edge profile templates of Figure 6, because it does not result in any change of the shape of the profile.

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R2-1.5 This is a very important point, because it shows that the only variation of the edge profile position in an actual wafer results from the wafer thickness and diameter variations.

R2-2 Constructing a Target Edge Profile

R2-2.1 Construct the target edge profile mathematically using the coordinates of each of the six reference points shown in Table R2-2. This table also gives the coordinates of the center points of the shoulder circular arcs.

R2-2.2 Construct the target profile as a cross-sectional view of the near-edge region of the wafer with the following coordinate system:

R2-2.3 The q-axis is along the reference line with the positive direction extending to the right.

R2-2.3.1 The z-axis is at the outer edge of the wafer and perpendicular to the reference line with the positive direction toward the front surface.

R2-2.3.2 The origin is at the intersection of the q- and z-axes.

Table R2-3 Coordinates of Target Edge Profile Reference Points and Shoulder Circle Center Points

Point	*Description (Moving Counterclockwise Around the Edge)*	*q-coordinate*	*z-coordinate*
A_f	Starting point of front bevel.	a_f	$t/2$
B_f	Ending point of front bevel, starting point of front shoulder.	$r_f(1-\sin\phi_f)$	$b_f + r_f\cos\phi_f$
M_f	Center point of front shoulder circular arc.	r_f	b_f
C_f	Ending point of front shoulder, starting point of front apex.	0	b_f
Origin	Origin of q-z coordinate system	0	0
C_b	Back point of apex, starting point of back shoulder.	0	$-b_b$
M_b	Center point of back shoulder circular arc.	r_b	$-b_b$
B_b	Ending point of back shoulder, starting point of back bevel.	$r_b(1-\sin\phi_b)$	$-(b_b + r_b\cos\phi_b)$
C_b	Ending point of back bevel.	a_b	$-t/2$

R2-2.4 Although the construction sequence does not affect the resulting target edge profile, use the following sequence or its reverse for the simplest construction procedure. For this example of a target edge profile, use the target values of the parameters listed in Table R3-1.

R2-2.4.1 Begin the construction of the target profile by drawing the front surface as a line through and to the right of reference point A_f parallel with the q-axis.

R2-2.4.2 Draw the front bevel from the reference point A_f to the reference point B_f; this line is at the front bevel angle ϕ_f with the front surface.

R2-2.4.3 Draw the front shoulder circular arc, of radius r_f and center M_f. This circular arc is tangent to the front bevel at the reference point B_f and tangent to the front apex at the reference point C_f.

R2-2.4.4 Draw the apex along the z-axis extending a distance b_f in the negative direction to the origin and continue a distance b_b in the negative direction from the origin to reference point C_b.

R2-2.4.5 Draw the back shoulder circular arc, of radius r_b and center M_b. This circular arc is tangent to the back apex at the reference point C_b and tangent to the back bevel at the reference point B_b.

R2-2.4.6 Draw the back bevel from the reference point B_b to the reference point A_b; this line is at the back bevel angle ϕ_b with the back surface.

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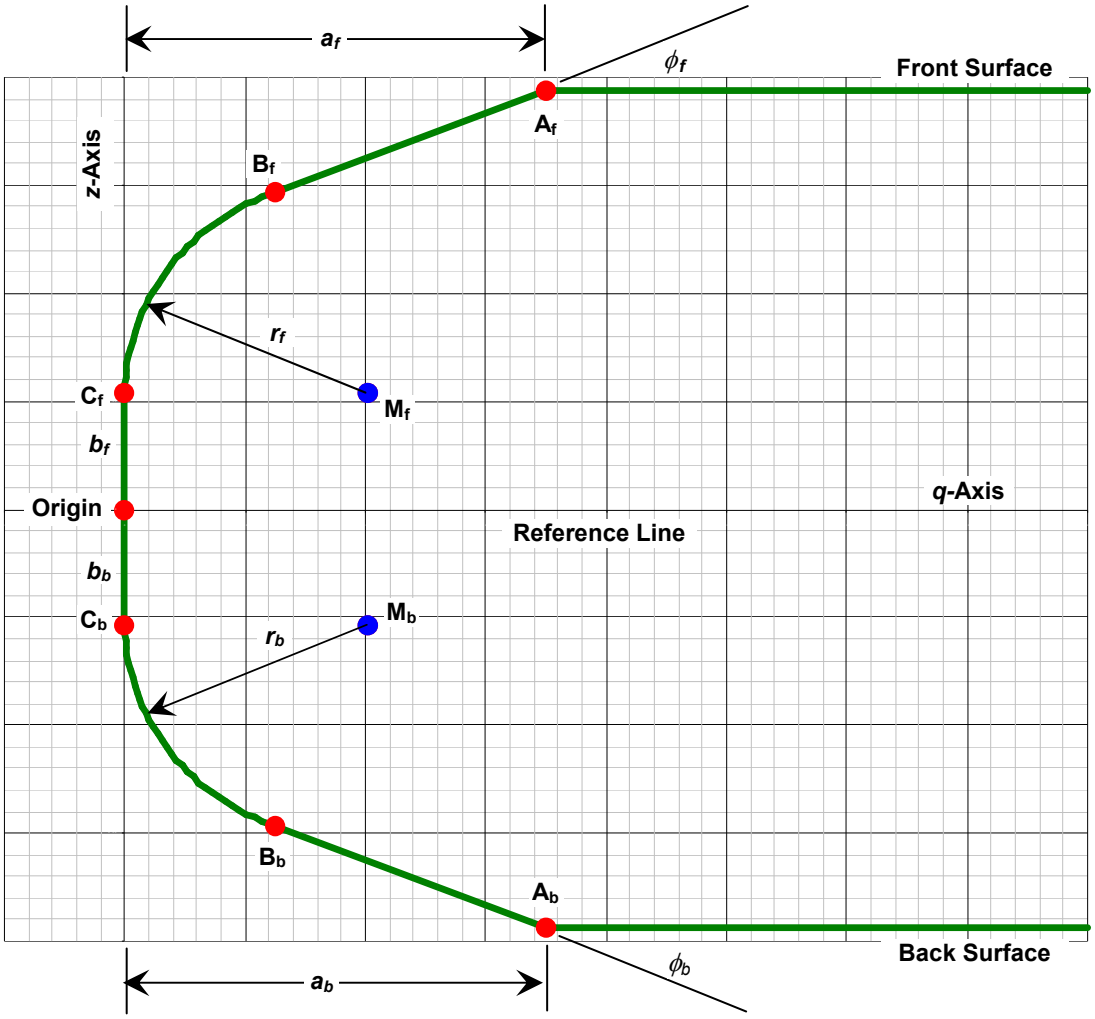
R2-2.4.7 Draw the back surface as a line through and to the right of the reference point A_b parallel with the *q*-axis.

R2-2.4.8 The completed target profile for the edge profile with the values specified in Table R3-1 is shown Figure R3-1.



NOTE: Because no sharp points are permitted on the edge profile, the actual profile on the wafer has a rounded transition between the edge and the wafer surface instead of the angular intersection shown in the target profile in this figure.

Figure R2-1

Example Target Profile for a 300 mm Diameter Notched Wafer

R2-3 Determining the Outline of Acceptable Profiles

R2-3.1 Construct nine profile curves using the limits of the specified parameters derived from Table R3-1 together with the target value of the specified wafer thickness. These parameters are listed in Table R3-4.

R2-3.2 In each case, calculate the value of the front and back apex lengths using Equations R3-1 and R3-2, respectively. These are also shown in Table R2-4 for 450 mm diameter wafers. Note that the apex lengths for 300 mm wafers are simply 75 mm less than those shown in the table.

R2-3.3 Again, use the sequence given in § R2-2 for the construction of the target profile.

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R2-3.4 As can be seen from Figure R2-2, curve H forms the inner boundary while curve A forms the outer boundary.

Table R2-4 Parameter Values for Limiting Edge Profile Curves on 450 mm Diameter Wafers

Parameter Name	*Symbol*	*Target*	*Curve A*	*Curve B*	*Curve C*	*Curve D*	*Curve E*	*Curve F*	*Curve G*	*Curve H*	*Unit*
Front edge width	a_f	350.00	300.00	300.00	300.00	300.00	400.00	400.00	400.00	400.00	µm
Front bevel angle	ϕ_f	22.5	19.5	19.5	25.5	25.5	19.5	19.5	25.5	22.5	deg
Front radius	r_f	202.50	160.00	245.00	160.00	245.00	160.00	245.00	160.00	245.00	µm
Front apex	b_f	182.22	243.19	183.12	218.45	164.82	207.78	147.70	174.05	117.13	µm
Back apex	b_b	182.22	243.19	183.12	218.45	164.82	207.78	147.70	174.05	117.13	µm
Back radius	r_b	202.50	160.00	245.00	160.00	245.00	160.00	245.00	160.00	245.00	µm
Back bevel angle	ϕ_b	22.5	19.5	19.5	25.5	25.5	19.5	19.5	25.5	25.5	deg
Back edge width	a_b	350.00	300.00	300.00	300.00	300.00	400.00	400.00	400.00	400.00	µm

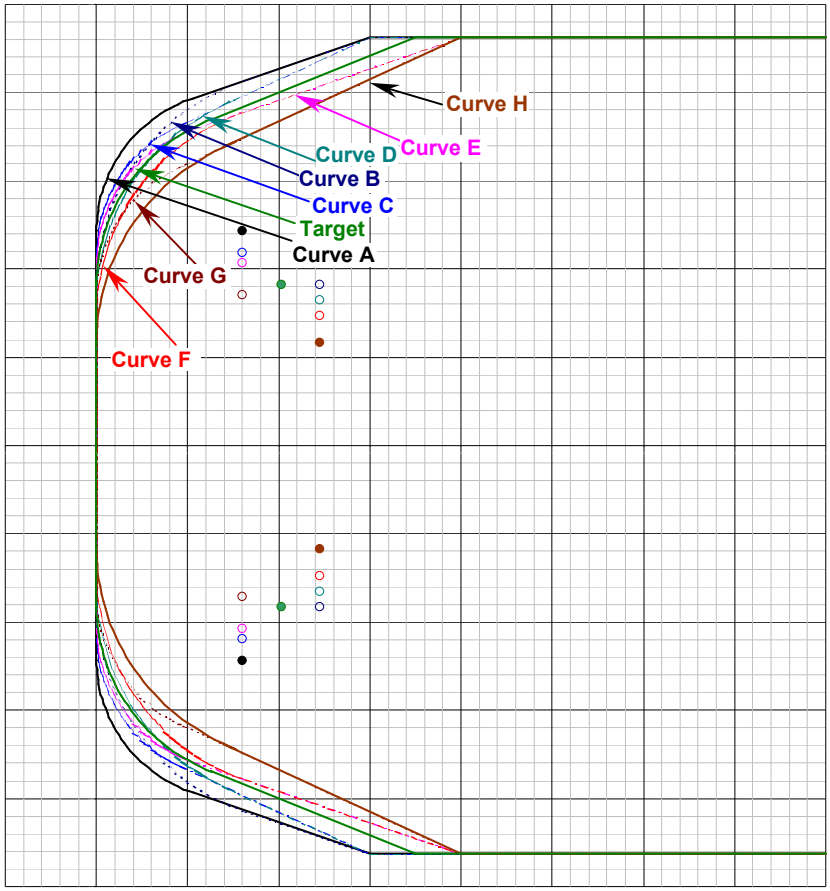

Figure R2-2
Limiting Edge Profile Curves for 450 mm Wafers

R2-3.5 Again, it should be emphasized that the only difference between the limiting curves for 300 mm and 450 mm wafers is the length of the front and back apexes when the bevel angles, edge widths, and shoulder radii are specified. When the apexes and two other parameters are specified, this is not necessarily the case, because in such cases, the shape of the profile may change when the parameter values change within their allowable ranges.

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R2-4 Form the Edge Profile Envelope

R2-4.1 Form the outer boundary of the profile envelope from curve A shifted 50 µm to the left (see Note 1).

R2-4.2 Form the inner boundary of the profile envelope from curve H shifted 50 µm to the right (see Note 1).

R2-4.3 The profile envelope for 450 mm wafers is shown in Figure R2-3.

NOTE 1: For 300 mm wafers the shift would have to be 100 µm to the left or to the right, as appropriate, because the diameter tolerance of 300 mm wafers is ±200 µm, while for 450 mm wafers it is ±100 µm. As a result the width of the envelope along the *q*-axis for 300 mm wafers would be 200 µm instead of 100 µm as shown in Figure R2-3.

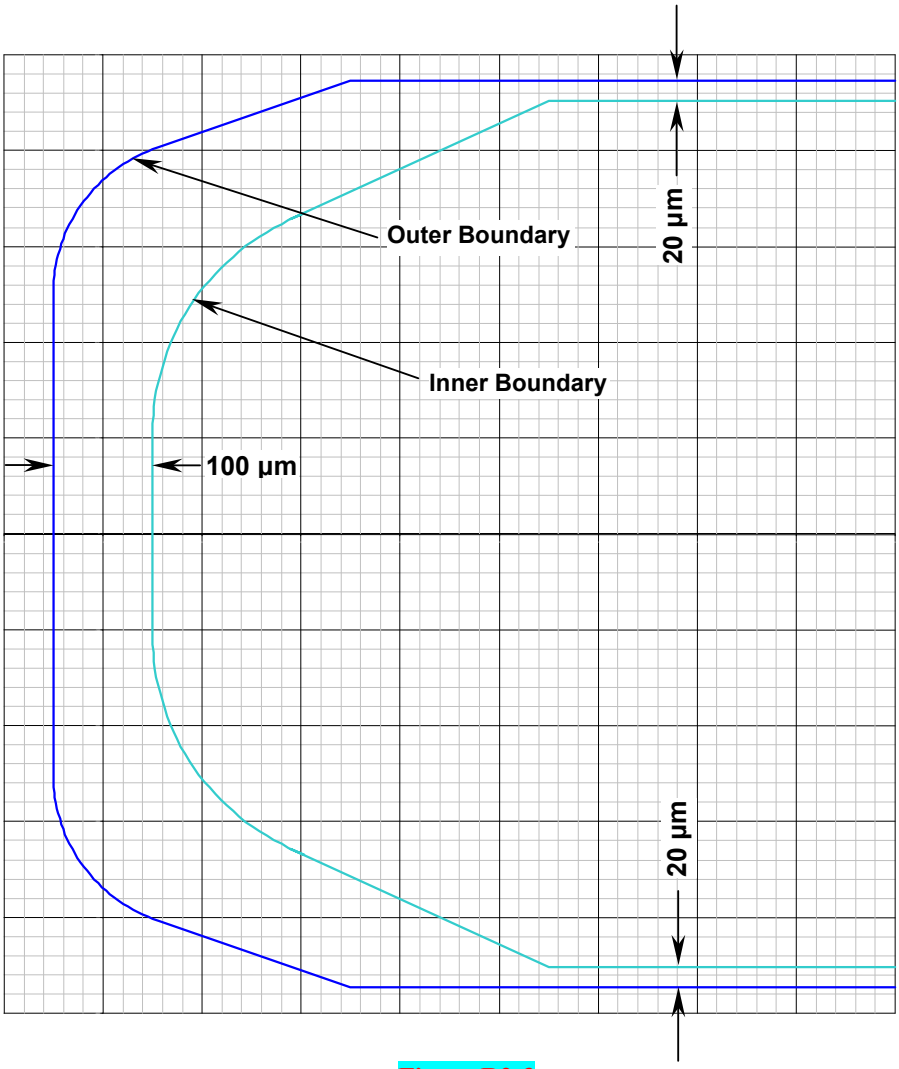

Figure R2-3
Example Edge Profile Envelope for 450 mm Wafers

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LETTER (YELLOW) BALLOT

RELATED INFORMATION 3 ~~RELATED INFORMATION 2~~
SURFACE METAL CONTAMINATION

NOTICE: This Related Information is not an official part of SEMI M1 and was derived from the work of the global Silicon Materials Technical Committee. This Related Information was approved for publication by full letter ballot beginning with the 1995 edition of the Standard.

~~R1-3~~ R3-1 ~~Scope~~Introduction

~~R1-3.1~~ R3-1.1 Maximum allowable surface metal contamination levels for wafers to be used in integrated circuit (IC) fabrication generally depend upon the IC device density and upon the IC process design. In general, as the device density increases, the allowable surface metal contamination levels become lower.

~~R1-3.2~~ R3-1.2 This Related Information is intended to provide guidance regarding allowable surface concentrations of metal contaminants that have been reported to be deleterious to circuit and device performance.

~~**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.~~

~~R1-4~~ R3-2 Suggested Allowable Surface Metal Contamination Levels for 1 µm Geometries

~~R1-4.1~~ R3-2.1 Table ~~R1~~R3-1 lists suggested surface metal limits for circuits and devices with a minimum linewidth in the range of 0.8 µm to 1.2 µm for two alkali metals (Na, K), a light metal (Al), and five heavy metals (Cr, Fe, Ni, Cu, Zn). These are same elements as are listed in the items under § 2-7 of Table 1, Part 2, and they are listed in the same order as they appear in that table.

~~R1-4.2~~ R3-2.2 Contaminant levels in Table ~~R2~~R3-1 are significantly higher than would be allowed for leading edge technologies at the time of approval of this standard.

~~R1-5~~ R3-3 Test Methods

~~R1-5.1~~ R3-3.1 The test methods suitable for use in determining the levels of each surface metal contaminant are listed in the items under § 2-7 of Table 1, Part 2. This list and the related discussion of these test methods in Related Information ~~3~~ 4 should be ~~referenced~~ used for guidance in selecting and specifying methods appropriate for testing the individual surface metals.

~~Table R1-2~~ Table R3-1 Suggested Polished Wafer Surface Metal Contamination Limits Appropriate to Circuits and Devices with a Minimum Linewidth in the Range 0.8 µm to 1.2 µm

Element	*Contaminant Level*
Sodium (Na)	Not greater than 1×10^{11} atoms/cm^2
Aluminum (Al)	Not greater than 1×10^{11} atoms/cm^2
Potassium (K)	Not greater than 1×10^{11} atoms/cm^2
Chromium (Cr)	Not greater than 1×10^{11} atoms/cm^2
Iron (Fe)	Not greater than 1×10^{11} atoms/cm^2
Nickel (Ni)	Not greater than 1×10^{11} atoms/cm^2
Copper (Cu)	Not greater than 1×10^{11} atoms/cm^2
Zinc (Zn)	Not greater than 1×10^{12} atoms/cm^2

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LETTER (YELLOW) BALLOT

~~RELATED INFORMATION 3~~RELATED INFORMATION 4
TEST METHODS

NOTICE: This Related Information is not an official part of SEMI M1 and was derived from the work of the global Silicon Wafer Technical Committee. This information was developed during the revision of this Standard in 2004. It is based in part on information previously published as part of SEMI M28, Withdrawn in October 2000. This Related Information was approved for publication by full letter ballot procedures on November 19, 2008.

~~R3-1~~ R4-1 ~~Scope~~Introduction

~~R3-1.1~~ R4-1.1 This Related Information section discusses aspects of the various test methods listed in Part 2 of Table 1 together with additional information about other test methods that are not listed in Table 1 but either have been or still are used in the industry. Note that these include the DIN test methods listed in the Related Documents section.

~~R3-1.2~~ R4-1.2 The next section contains references to the test methods that are not cited in the main body of SEMI M1 but that are discussed here. The various test methods are discussed in order that the items they cover are listed in Table 1.

~~R3-1.3~~ R4-1.3 Note that silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must, therefore, be used in the selection and execution of measurement methods.

~~**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.~~

~~R3-2~~ R4-2 Referenced Standards and Documents

~~R3-2.1~~ R4-2.1 The standards listed in this section are referenced only in this Related Information. See §3 ~~-6~~ for other standards that are referenced in this Related Information.

~~R3-2.2~~ R4-2.2 *SEMI Standards*

SEMI M49 — Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 22 nm Technology Generations

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm~~, 90 nm, 65 nm, and 45~~ to 11 nm Technology Generations

SEMI MF43 — Test Methods for Resistivity of Semiconductor Materials

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavenumber or Wavelength of the Plasma Resonance Minimum

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon

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SEMI MF1527 — Guide for Application of Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

SEMI MF1529 — Test Method for Sheet Resistance Uniformity Evaluation by In-Line Four-Point Probe with the Dual-Configuration Procedure

SEMI MF1618 — Practice for Determination of Uniformity of Thin Films on Silicon Wafers

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

~~R3-2.3~~ R4-2.3 *ANSI Standard*[1]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

~~R3-2.4~~ R4-2.4 *ISO Standards*[5]

ISO 4287-1 — Surface Roughness – Terminology – Part 1: Surface and Its Parameters

ISO 14644-1 — Clean Room and Associated Controlled Environments – Part 1: Classification of Air Cleanliness

~~R3-2.5~~ R4-2.5 *JEITA Standard*[6]

JEITA EM-3505 — Height Calibration in 1 nm Order for AFM

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

~~R3-3~~ R4-3 General Characteristics

~~R3-3.1~~ R4-3.1 *Crystal Orientation* — The crystallographic orientation of the source crystal can be determined by the x-ray methods of SEMI MF26, JEITA EM-3501, or DIN 50433-1, the optical method of SEMI MF26 or DIN 50433-2, or the Laue method of DIN 50433-3. X-ray methods are most commonly used by wafer suppliers.

~~R3-3.2~~ R4-3.2 *Conductivity Type* — One of the five methods of SEMI MF42, one of the methods of JIS H 0607, or one of the four methods of DIN 50432 should be used to determine conductivity type. This quantity is generally well controlled by silicon wafer suppliers and is not usually verified on incoming.

~~R3-3.3~~ R4-3.3 Many of these tests need to be carried out in cleanroom environments of ISO Class 4, 5, or 6 depending on the cleanliness requirements. These classes are defined in ISO 14664-1.

~~R3-4~~ R4-4 Electrical Characteristics

~~R3-4.1~~ R4-4.1 *Resistivity* — The resistivity of wafers is most appropriately determined for referee purposes by SEMI MF84 or DIN 50431. Under some circumstances these tests may be considered destructive, and an alternative means may be required. One nondestructive test is SEMI MF673, having a range from 0.0001 to 100 Ω·cm. Another nondestructive test is SEMI MF398, which is limited to carrier concentrations in the ranges from 1.5×10^{18} to 1.5×10^{21} cm^{-3} for *n*-type silicon and from 3×10^{18} to 5×10^{20} cm^{-3} for *p*-type silicon, and has only moderate inter-laboratory precision. Other older methods that require a bar-shaped test specimen include SEMI MF43 and DIN 50430; these methods are no longer in general use. It is also possible to establish the dopant density from room temperature measurements in silicon using SEMI MF723 (for boron, phosphorus, or arsenic doped silicon) or DIN 50444 (for boron and phosphorus doped silicon only). SEMI MF1527 is a useful standard in describing ways of ensuring that resistivity measuring instruments are performing correctly.

~~R3-4.2~~ R4-4.2 *Radial Resistivity Variation* — The radial resistivity of wafers is generally determined by SEMI MF81 or DIN 50435. These test methods use several different measurement positions so the desired position

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must be specified. It is also possible to measure the resistivity in one of the circular patterns specified in SEMI MF1618 using SEMI MF1529 as the resistivity measurement method.

~~R3-4.3~~ R4-4.3 *Resistivity Striations* — One of the techniques discussed in § R2-9 can generally be used to visually view resistivity striations. For an electrical measurement, spreading resistance (SEMI MF525) is generally employed but this is strictly an off-line measurement.

~~R3-4.4~~ R4-4.4 *Minority Carrier Lifetime* — A number of methods can be used to measure minority carrier lifetime. The photoconductive decay methods (SEMI MF28, JIS H 0604, and DIN 50440-1) all require the use of special test specimens; Microwave reflectivity measurements (SEMI MF1535 and JEITA EM-3502) are applicable to measurements on wafers, but special surface passivation procedures may be required to obtain meaningful results. Minority carrier lifetime may also be inferred from measurements made in accordance with SEMI MF1388, which yields generation lifetime if the measurements are made at room temperature and recombination lifetime if they are made at elevated temperature (50°C to 75°C). The test specimens required for this test method can be made by procedures compatible with typical wafer processing.

~~R3-5~~ R4-5 Chemical Characteristics

~~R3-5.1~~ R4-5.1 *Oxygen Concentration* — In relatively high resistivity specimens (ρ >1 to 3 Ω·cm at room temperature) should be measured by infrared techniques. SEMI MF1188, JEITA EM-3504, and DIN 50438 all utilize approximately normal incidence illumination and the IOC-88 calibration factor to determine the interstitial oxygen content. See SEMI M44 for a discussion of other calibration factors and their relationship to IOC-88. SEMI MF1619 uses *p*-polarized radiation, incident at the Brewster angle to reduce the multiple reflections from polished wafers. For more heavily doped wafers, secondary ion mass spectrometry (SIMS, SEMI MF1366) and gas fusion analysis (GFA) can be used to determine total oxygen content. There is no standardized method for performing GFA, and the repeatability of this technique is generally poorer than SIMS.

~~R3-5.2~~ R4-5.2 *Radial Oxygen Variation* — The radial variation of oxygen should be determined by measuring the oxygen content by one of the above methods at selected locations on the wafer defined in SEMI MF951. Usually measurements are made at the center and at a single point on the primary flat or notch bisector 10 mm from the edge of the wafer opposite the fiducial; this is known as test plan A-1.

~~R3-5.3~~ R4-5.3 *Carbon Concentration* — The carbon concentration should be measured by SEMI MF1391, JEITA 56, or DIN 50438-2. The most modern calibration coefficients are used in SEMI MF1391 and JEITA 56. For these methods, the test specimen cannot be too heavily doped, and special thick test specimens may be necessary.

~~R3-5.4~~ R4-5.4 *Boron Contamination* — In heavily doped *n*-type silicon, boron contamination can be determined by SEMI MF1528.

~~R3-5.5~~ R4-5.5 *Bulk Iron Content* — The bulk iron content can be determined by deep level transient spectroscopy in accordance with SEMI MF978. Under certain conditions it can be determined from surface photovoltage measurements made in accordance with SEMI MF391; however, interpretation of the presence of iron or other contaminants by this test method is outside the scope of the Standard. Also, under certain conditions, iron content has been proposed to be determined from microwave lifetime measurements; the effects of iron content on such measurements are discussed in some detail in SEMI MF1535 together with literature citations to the technical papers proposing such determinations.

~~R3-6~~ R4-6 Structural Characteristics

~~R3-6.1~~ R4-6.1 *Dislocation Etch Pit Density, Slip, Lineage, Twins, and Swirl* — These defects are usually displayed by etching and visual or microscopic observation. JIS H 0609 is a comprehensive test method for carrying out this procedure with the use of non-chromic etchants. SEMI MF1809 also recommends non-chromic etchants for this test. For the full procedure, SEMI MF1809 must be used with other standards including SEMI MF1726 and SEMI MF1810. DIN 50434 is an older, but comprehensive test procedure to observe these and other structural

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defects based on chrome-containing etchants. It is also possible to observe these defects by X-ray topography using DIN 50443-1.

~~R3-6.2~~ R4-6.2 *Shallow Pits* — Shallow pits can be exposed by the relatively low temperature heating cycle and procedures in SEMI MF1049 if they are present in sufficient density, but testing for shallow pits in production environments is usually carried out using the temperature cycle in SEMI MF1727 followed by etching with etchants discussed in SEMI MF1809, examination by SEMI MF1726, and counting by SEMI MF1810. They can also be observed by using JIS H 0609.

~~R3-6.3~~ R4-6.3 *Oxidation Induced Stacking Faults* (*OISF*) — OISF can be observed by using JIS H 0609, or by using the temperature cycle in SEMI MF1727 followed by etching with etchants discussed in SEMI MF1809, examination by SEMI MF1726, and counting by SEMI MF1810. OISF can also be observed by X-ray topography using DIN 50443-1 following thermal treatment according to JIS H 0609 or SEMI MF1727.

~~R3-6.4~~ R4-6.4 *Oxide Precipitates* (*Bulk Micro Defects*, *BMD*) — These defects are generated with the use of a temperature cycle such as those in SEMI MF1239. The amount of precipitation can be measured by the oxygen reduction method of SEMI MF1239 or by direct observation by infrared that has not yet been standardized. The density of bulk micro defects can be measured by JEITA EM-3508. The width of a denuded zone can also be measured using JEITA EM-3508.

~~R3-6.5~~ R4-6.5 *Bulk Defects* — X-ray topography can be used in accordance with DIN 50443-1 to detect bulk defects.

~~R3-7~~ R4-7 Dimensional Characteristics

~~R3-7.1~~ R4-7.1 *Diameter* — In silicon wafers that have been edge profiled with cam follower equipment the diameter is presently very well controlled. Three-point measurements of diameter can be made at locations defined by SEMI MF2074 and, except for positions on 150 mm diameter, *n*-type (100) wafers, by DIN 50441-4. The latter utilizes a measuring or projection microscope to make the diameter measurements, but the former allows a dial gauge or any other equally accurate method of dimensional measurement.

~~R3-7.2~~ R4-7.2 *Flat Length* — SEMI MF671 should be used to determine flat length. If flat diameter is specified instead of flat length, it can be determined by ¶ 6.2.1 of DIN 50441-4 or by a dial gauge method as agreed upon between the supplier and customer. Both SEMI MF671 and DIN 50441-4 take account of the possibility that the ends of the flat might be rounded.

~~R3-7.3~~ R4-7.3 *Notch Dimensions* — Notch dimensions should be determined by SEMI MF1152 (see Figure 5).

~~R3-7.4~~ R4-7.4 *Flat Orientation* — Flat orientation can be confirmed by SEMI MF847. There is no standardized method for determining the crystallographic orientation of the diameter that bisects the notch.

~~R3-7.5~~ R4-7.5 *Edge Profile* — When specified by a T/3 or T/4 template, conformance of the edge profile is usually determined by using one of the two templates (see Figure 6) with Method B of SEMI MF928 or Procedure 2 of DIN 50441-2, both of which are nondestructive. The other two procedures in these methods are destructive and not so widely used. When parameters are specified, either of the test methods in SEMI M73 should be used. These two test methods utilize different fitting locations and procedures so that the results obtained for specific parameters would not be expected to agree with each other so it is critical for the test method to be agreed upon between supplier and customer. ~~Alternatively, the measured profile should be compared in accordance with § A3-4 to a parameter-based template constructed in accordance with § A3-3.~~

~~R3-7.6~~ R4-7.6 *Thickness* — Wafer thickness is usually determined at the center point of the wafer with the use of SEMI MF1530, an automated technique. Manual techniques originally used in the industry include SEMI MF533, JIS H 0611, and DIN 50441/1.

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~~NOTE 2:~~NOTE 1: Test methods SEMI MF1530 (for thickness, thickness variation, and flatness), SEMI MF1451 (for sori), and SEMI MF1390 (for warp) may not be suitable for use on large diameter wafers with polished back surfaces. New standardized test methods for measuring these parameters on such wafers have been ~~under~~ considered for development for some time.

~~R3-7.7~~ R4-7.7 *Total Thickness Variation* (*TTV*) — TTV was originally determined with the use of manual 5-point techniques covered in SEMI MF533, JIS H 0611, and DIN 50441-1. JIS H 0611 differs from SEMI MF533 and DIN 50441/1, in that the measurements in JIS H 0611 are taken at the center and at 5 mm from the edge on diameters parallel and perpendicular to the primary flat or notch bisector, while the measurements in SEMI MF533 and DIN 50441-1 are taken at the center and at 6 mm from the edge either on the diameters parallel and perpendicular to the primary flat or notch bisector or on diameters 30° and 120° counterclockwise from the bisector to the primary flat or notch (with the wafer facing front surface up). TTV can also be determined with the use of SEMI MF657, which involves a continuous scan pattern over a portion of the wafer surface. Currently, however, it is most frequently determined using SEMI MF1530, which involves an automated continuous scan pattern over the entire wafer surface. In this case, the quantity determined is equal to the global flatness GBIR (see Appendix 1 ~~and Note 9, above~~).

~~NOTE 3: SEMI MF533 is being modified to include five- or nine-point measurements on the diameters parallel and perpendicular to the primary flat or notch bisector.~~

~~R3-7.8~~ R4-7.8 *Surface Orientation* — The X-ray methods of SEMI MF26, JEITA EM-3501, or DIN 50433-1, the optical method of SEMI MF26 or DIN 50433-2, or the Laue method of DIN 50433/3 can be used to determine surface orientation.

R4-7.8.1 ~~R3-7.8.1~~ For off-orientation {111} wafers, the orthogonal misorientation may be specified (see line 2-1.9 of Table 1, Part 2). There is no standardized measurement method for this property so it should be determined by a method agreed upon between supplier and customer.

~~R3-7.9~~ R4-7.9 *Bow* — Bow can be determined with the manual methods SEMI MF534 and JIS H 0611. Currently, bow is not as widely used a parameter as warp.

~~R3-7.10~~ R4-7.10 *Warp* — Warp is currently most often measured with the use of SEMI MF1390, which is an automated method with full surface scan and correction for gravitational sag. It can also be measured with the use of the contactless manual method SEMI MF657, in which the prescribed scan pattern covers only a portion of the wafer surface in which there is no correction for gravitational sag. As noted in Appendix 2, different reference planes are used for the two methods. Because SEMI MF657 employs a back surface reference plane, the measured warp may include contributions from thickness variation of the wafer. SEMI MF1390 employs a median surface reference plane and is not susceptible to interferences from thickness variations. In general, the latter is preferred, especially for wafers 150 mm in diameter and larger (see Note 6, above).

~~R3-7.11~~ R4-7.11 *Sori* — Sori, which is sometimes specified in lieu of bow or warp or both, can be determined by SEMI MF1451 (see Note 6, above).

~~R3-7.12~~ R4-7.12 *Global Flatness* — Global flatness can be determined by either capacitance measurements, as in SEMI MF1530, or by multiple beam interference, as in DIN 50441-3. Generally, the former is considered to be more reliable, especially as the need increases for measuring smaller flatness deviation (see Note 6, above). As noted in ¶ R2-7.7, GBIR is the same as TTV; other global flatness parameters are discussed in Appendix 1.

~~R3-7.13~~ R4-7.13 *Site Flatness* — Site flatness is generally determined by SEMI MF1530 (see Note 6, above). The most commonly used site flatness parameter is SFQR; other site flatness parameters are discussed in Appendix 1. Although it is not widely used, the scanning site flatness parameter SFSR was recently introduced. For this parameter, use a subsite width, W_{ss}, equal to 8 mm and orient the wafer so the effective scan direction is along the wafer's *y*-axis as defined in SEMI M20.

R4-7.13.1 SEMI M49 is a guide for specifying test equipment for use in determining thickness, shape, and flatness parameters on wafers intended to be used to fabricate advanced integrated circuits.

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~~R3-7.14~~ R4-7.14 *Nanotopography* — SEMI M43 gives a variety of options that can be used for measurement of nanotopography, so it is essential to specify the various conditions that are desired in any given case. The conditions chosen should be agreed upon between supplier and customer.

~~R3-7.15~~ R4-7.15 *Near Edge Geometry* — There are four classes of metrics for characterizing the near edge geometry of the wafer.

~~R2-7.15.1~~ R4-7.15.1 SEMI M67 quantifies the flatness aspects of the near edge geometry using the one or more of the flatness metrics, EFSQR, EFSQD, or ESBIR over sectors at the outer edge of the FQA.

~~R2-7.15.2~~ R4-7.15.2 SEMI M68 quantifies the radial curvature, ZDD, of wafers in the near edge region.

~~R2-7.15.3~~ R4-7.15.3 SEMI M77 quantifies the roll-off amount, ROA, based on a linear reference, (L-ROA) or a polynomial reference (P-ROA) in the near edge region.

~~R2-7.15.4~~ R4-7.15.4 SEMI M70 quantifies the wafer flatness using partial sites at the outer edge of the FQA. The metrics are PSFQR or PSFQD.

~~R3-8~~ R4-8 Front Surface Chemistry

~~R3-8.1~~ R4-8.1 *Surface Metal Contaminants*

R4-8.1.1 Sodium, aluminum, potassium, and iron can be measured by secondary ion mass spectrometry (SIMS), inductively coupled plasma mass spectrometry (ICP/MS), or atomic absorption spectroscopy (AAS). SIMS has been standardized as SEMI MF1617. The latter two methods are frequently combined with vapor phase decomposition (VPD), but they have not yet been standardized.

R4-8.1.2 Potassium, chromium, iron, nickel, copper, and zinc can be measured by total reflection x-ray fluorescence spectroscopy (TXRF), ICP/MS, and AAS. TXRF has been standardized both with (SEMI M33 and ISO 17706) and without (ISO 14706) use of VPD to preconcentrate the surface metal contaminants.

R4-8.1.3 VPD is chemical preconcentration of the surface metals using vapor phase HF to decompose the surface native oxide and a water (or acid-spiked water) droplet to scan across the wafer dissolving the surface metals. The recovery rate of this preconcentration method is dependent upon the chemistry of the surface metals and upon the chemistry used for the preconcentration. An alternative preconcentration method to VPD is to scan an acid droplet across the wafer surface.

R4-8.1.4 VPD/AAS is a single-element technique which is widely used in Japan. It is element-specific and very sensitive. VPD/ICP-MS is a rapid multi-element technique which is a more recent development. It is also very sensitive, but its reproducibility is dependent upon the injection process into the ICP-MS. VPD/TXRF is an even more recently developed multi-element technique. It is also very sensitive, but its reproducibility is dependent on the residue-drying process.

~~R3-8.2~~ R4-8.2 *Surface Organics* — Surface organics can be measured by SEMI MF1982. This Standard describes two methods; the method to be utilized should be agreed upon between supplier and customer.

~~R3-9~~ R4-9 Surface Inspection Characteristics

~~R3-9.1~~ R4-9.1 *Visual Inspection* — Either the front or back surface of wafers can be visually inspected in accordance with SEMI MF523 or JIS H 0614. The following conditions should be used for examination under high intensity illumination:

- Background light intensity: 8 ± 2 fc (86 ± 22 lux),

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- Angle (alpha): 45° ± 10°, and
- Angle (beta): 90° ± 10°.

See ¶ 6.8 and subsequent paragraphs for a discussion of which artifacts on the surface should be considered as defects. SEMI MF154 is a useful guide for identifying structures and contaminants seen on silicon surfaces.

R4-9.1.1 *Scratches* — In inspecting for scratches, it is important to note that while macro-scratches can be seen under both high intensity and diffuse illumination, micro-scratches can be seen only under high intensity illumination. Therefore, to separate the two kinds of scratches, it is necessary to count the scratches observed under both kinds of illumination. The count of scratches seen under diffuse illumination is the number of macro-scratches while the difference of the counts seen under high intensity illumination and diffuse illumination is the number of micro-scratches. Of course, if the total requirement is for no scratches of either kind, then examination under high intensity illumination only is adequate.

~~R3-9.2~~ R4-9.2 *X-ray Topography (DIN 50443-1)* — This method may see defects that do not intersect the surface, and can also be used to examine for bulk defects in the wafer (see row 2-4.10 of Table 1).

~~R3-9.3~~ R4-9.3 *Automated Surface Inspection by Light Scattering* — Many surface defects, especially on polished surfaces, can be detected with automated surface inspection techniques based on light scattering. These techniques have not been fully standardized, but there is a group of standards that assist in making certain that the instruments are performing correctly. These include SEMI M52 for determining if surface scanning inspection systems (SSIS) have suitable characteristics for the desired use, SEMI M53 for calibrating SSISs, SEMI M58 for assuring that the calibration artifacts meet the desired requirements, SEMI M50 for determining capture rate characteristics of SSISs and SEMI M35 for discriminating among various surface features with an SSIS. Because of the lack of complete standardization, the testing conditions for use of SSISs should be agreed upon between supplier and customer.

R4-9.3.1.1 *Localized Light Scatterers* — SSISs are particularly appropriate for inspecting polished surfaces for the presence of particles and other localized light scatterers (LLS). In this case, it is essential to define the size ranges (in units of latex sphere equivalents, LSE) as well as the maximum permissible counts, usually in terms of counts per wafer, but occasionally in terms of counts per unit area.

~~NOTE 4:~~NOTE 2: A table relating counts per wafer to counts per square meter and counts per square centimeter is given in SEMI M62.

~~R3-9.4~~ R4-9.4 *Surface Roughness* — The size of particle or other LLS that can be detected on a surface is affected by the surface roughness. SEMI M40 provides guidance on how to measure and report surface roughness on planar surfaces. Surface microroughness can be determined with SSISs, through the use of the power spectral density as described in SEMI MF1811, or with an atomic force microscope, which can be calibrated with the use of JEITA EM-3505. Other standards useful in connection with surface microroughness measurements include ISO 4287-1 and ANSI/ASME B46.1. Because of the lack of standardization, the testing conditions for surface microroughness measurements should be agreed upon between supplier and customer.

~~NOTE 5:~~NOTE 3: SEMI MF1048 provides a standardized way of determining surface rms microroughness over a defined spatial bandwidth range.

~~R3-9.5~~ R4-9.5 *Back Surface Finish* — The back surface of 300 mm diameter wafers specified as “polished” is not as smooth as the mirror polished front surface. The standard quantitative test for the back-surface polish is gloss. The general techniques for determining gloss are given in ASTM D523 and JIS Z 8741. However, for measuring gloss of silicon surfaces, visible illumination at a 60° angle of incidence is referenced to a mirror polished silicon front surface. Surface microroughness measurements (see ¶ R2-9.4) can also be used as a quantitative test for back surface finish, especially when it is necessary to observe particles or other LLSs smaller than 0.25 µm LSE on the surface.

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REVISION RECORD

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Cycle	*Authorization*	*Section*	*Description*
0305	Ballot 3907	Entire Document	This revision combines most of SEMI M1 with parts of SEMI M18 to form a new set of specifications that includes: Purpose, a new scope, referenced standards, ordering information (consolidated with some of SEMI M18), requirements (assembled from several existing sections in SEMI M1), sampling, test methods, certification, and packing and shipping container labeling sections; Basic polished wafer specifications (developed by the Basic Wafer Specification TF); The two Appendices and one Related Information section included in previous editions of SEMI M1; and A new Related Information section on detailed discussion of test methods, based largely on material previously in SEMI M28. A new table of contents has been added to make it easier to locate specific information in the Standard, and the terminology section of SEMI M1 was combined with SEMI MF1241 and issued as SEMI M59. The EDI codes from SEMI M18 remain in that Standard. The material in all of the substandards previously included at the end of SEMI M1 is now included in the body of the document with no change of the technical content. In addition, polished wafers and substrates have been assigned category numbers based on the previous substandard designation number. In some cases there are two categories, based on differences in the edge rounding template used. All of the specification requirements previously in the substandards have been moved to tables as follows:

Substandard	*Nominal Diameter*	*Located in Table*	*Wafer Category(s)*
SEMI M1.1	2 inch	4	1.1
SEMI M1.2	3 inch	4	1.2
SEMI M1.5	100 mm	5	1.5
SEMI M1.6	100 mm	5	1.6
SEMI M1.7	125 mm	5	1.7
SEMI M1.8	150 mm	6	1.8.1 and 1.8.2
SEMI M1.9	200 mm	9	1.9.1 and 1.9.2
SEMI M1.10	200 mm	8	1.10.1 and 1.10.2
SEMI M1.11	100 mm	7	1.11
SEMI M1.12	125 mm	7	1.12
SEMI M1.13	150 mm	8	1.13.1 and 1.13.2
SEMI M1.15	300 mm	9	1.15

Additional material related to 300 mm wafers is given elsewhere in SEMI M1, most notably in ¶ 6.5.1.4, which describes the wafer marking requirements. Also it should be noted that (1) the information on surface orientation, for which the substandards allowed any of a number of options, has been moved to Item 2-1.8 of Table 1, Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, and (2) the information on orthogonal misorientation, which is the same for all (111) silicon wafers has been moved to Item 2-1.9 of the same table.

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Cycle	*Authorization*	*Section*	*Description*
1106	Ballot 4281	§ 7, Table 8, and Table 13	Information and tables being considered for change in Document 4281 was last revised as Document 3907 in July 2004. § 7 and Table 12 of SEMI M1 has become generally known as the Basic Wafer Specification. Several changes and enhancements were recommended at the San Francisco and Tokyo Silicon Wafer Committee meetings in 2005. Agreement was reached to ballot the suggested line items at the NA Silicon Wafer Committee meeting in Denver in March 2006. Changes to the titles and table description are offered to better explain the Non-optional character of the Basic Wafer and to remove the association of the Basic Wafer Specification to a specific device node. The sense of the committee is that the basic wafer should not change with the industry node. Format Alignment - Item names were changed for Fiducial Dimension and Primary Flat / Notch Orientation to align with M18. Clarification of the specification for site flatness as being based on shipment sized quantities of site measurements rather than based upon individual wafer based site distributions. The definition of micro scratches needed clarification to allow integration into SSIS tool recipes. The tolerance of center point thickness for 200 mm wafer (without secondary flat) was added to be consistent with table 9, which specifies 725 ± 20 μm for 200 mm notched wafer.
0307	Ballot 4273	§ 3, § 6, and Appendix 3	§ 3.8, ¶ 6.3.2, and Appendix 3 were added to introduce RoHS requirements for silicon wafers.
0707	Ballot 4422	§ 5, § 6, and Table 1	Changes were made to ¶ 5.4.3, ¶ 6.1.5, ¶ 6.1.5.1 and Item 2-6.2 of Table 1.
0309	Ballot 4620	Throughout	This revision involves the following parts of SEMI M1 dealing with edge profile specifications: Changes in ¶¶ 2.2 (addition of two new wafer categories), 3.1 (addition of test methods reference), 6.6.2 through 6.6.2.4, and R2-7.5; Changes in § 2-6.6 of Tables 1 and 9 (renumbered 10); and Addition of Appendix 3, Target-Based Template for Parameter-Specified Edge Profiles. In addition, several errors in the published text have been corrected, and the Appendices have been rearranged so that that they are numbered in the order they are referenced in the text of the Standard.
1109	Ballot 4732	§ 3, Table 1, § 6, and Related Information 2	¶ 3.1: Title correction and new documents added. Table 1: Row 2-6.15 added. ¶ 6.3.2 revised, Note 1 added, ¶ 6.6.7 added. Related Information 2: ¶¶ R2-7.15-R2-7.15.4 added.
0211	Ballot 4927, Line Items 1–3	Throughout	Changes were made throughout the document.
0611	Ballot 5133, Line Items 1–2	§ 2.6, § 3, § 4.1, Table 1, and § R2-7	Line Item 1 covers some updates that result from revisions of cited standards and a few other editorial and style issues. Line Item 2 covers some updates on withdrawn SOI Wafer references.
1011	Ballot 5090	Throughout	Changes made to ¶¶ 2.2, 5.7, and Table. Addition of Note 5 and Table 11.

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