Background Statement for SEMI Draft Document 5175
NEW STANDARD: GUIDE FOR MULTI-WAFER TRANSPORT AND STORAGE CONTAINERS FOR 300 mm, THIN SILICON WAFERS ON TAPE FRAMES

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Background

This document was written by the Thin Wafer Handling Task Force of the 3DS-IC Committee to provide the 3DS-IC community with the tools needed to ship thin wafers for use with 3D stacking applications. For the last few decades semiconductor industry has been following Moore Law effectively, which has resulted in significant miniaturization of transistors and on chip logic circuitry. Below the 28nm node, as design complexity of the IC (Integrated Circuits) increases, cost and risk associated with these designs could become prohibitive for many companies. Three dimensions (3D) die stacking methodology offers unique advantages of low power and high bandwidth per watt without increasing the cost significantly. Majority of the semiconductor industry has been evaluating various approaches to integrate different ICs on active or passive interposers. Some of these solutions are already being used in product, albeit at relatively low volumes compared to standard assembly techniques such as wire bond and flip chip assembly.

However, as the market need for 3D IC grows and complexity of the supply chain will increase and thin silicon wafers (50 µm to 200 µm), active or passive, will have to be moved from one location to the other for assembly. Currently there is limited data available from initial products that have been launched in the last few years and there is a need to establish minimum guidelines to ship such delicate wafers without creating any defects during shipment.

This document was developed in the Thin Wafer Handling TF of N.A. 3DS-IC Committee. The SNARF for this was approved March 29, 2011. Draft Document 5175 was approved for yellow ballot in Cycle 1 in CY2013, by the N.A. 3DS-IC Committee on October 30, 2012.

Review and Adjudication Information

	Task Force Review	Committee Adjudication
Group:	Thin Wafer Handling Task Force	NA 3DS-IC (Three-dimensional Stacked Integrated Circuits) Technical Committee
Date:	Tuesday, April 2, 2013	Tuesday, April 2, 2013
Time & Timezone:	8:00 AM to 10:00 AM, Pacific Time	3:00 PM to 5:00 PM, Pacific Time
Location:	SEMI HQ	SEMI HQ
City, State/Country:	San Jose, California	San Jose, California
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This meeting's details are subject to change, and additional review sessions may be scheduled if necessary. Contact Standards staff for confirmation.

Telephone and web information will be distributed to interested parties as the meeting date approaches. If you will not be able to attend these meetings in person but would like to participate by telephone/web, please contact Standards staff.

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LETTER (YELLOW) BALLOT

SEMI Draft Document 5175
NEW STANDARD: GUIDE FOR MULTI-WAFER TRANSPORT AND STORAGE CONTAINERS FOR 300 mm, THIN SILICON WAFERS ON TAPE FRAMES

1 Purpose

1.1 This guide is intended to address the needs for choosing a method for shipping thin wafers on tape frames in such a way that they arrive undamaged at their final destination. It describes various methods of shipping thin wafers on tape frames.

1.2 Shipping thin wafers without damage requires the use of appropriate transport and storage containers because of several interacting factors, the most important of which are listed here.

1.2.1 Although the thicknesses of standard wafers have increased with increasing diameter due to increased fragility with dimension, process flows for three-dimensional stacked ICs (3DS-ICs) reverse that trend, using thinned, and hence much more fragile, wafers to allow for shorter through-wafer interconnects and lower total volume of the stack.

1.2.2 Stacking processes, especially for heterogeneous integration, will necessitate the use of wafers from multiple sources, which means that the wafers must be shipped from location to location.

1.2.3 A package dropped from a height of approximately 1 meter will experience an impact on the order of 100 g. Such an event is easily capable of breaking a wafer that is not properly protected.

2 Scope

2.1 This guide provides the user with information about containers needed to ship thin wafers that are mounted on dicing tape to tape frames conforming to either SEMI G74 or SEMI G87.

2.2 This guide covers the shipping of 300 mm nominally diameter silicon wafers. The actual diameter of a 300 mm (nominal) silicon wafer may be less than 300 mm due to material removal via edge trim; the diameter of 300 mm silicon wafers fabricated specifically for use as carrier wafers may be greater than 300 mm.

2.2.1 The maximum diameter of a nominal 300 mm wafer is 301 mm

2.2.2 There is not a fixed minimum diameter for nominal 300 mm wafers; edge trim and other processes are not yet standardized; thus, the actual diameter of nominal 300 mm wafers may millimeters smaller

2.3 This Guide may be useful for materials other than silicon, but that is beyond the scope of this document.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This guide does not purport to describe methods for shipping thinned wafers that are mounted or held in any manner other than on dicing tape, on tape frames.

3.2 This guide does not purport to describe methods for shipping wafers of diameter other than 300 mm (nominal), for example 200 mm or 450 mm.

3.3 The laboratory experimental results described in this document (Appendix 1) were performed on wafers 50 µm and 100 µm thick. The methodology can be applied to other thicknesses, but use of these shipping methods on wafers with other thicknesses is outside to scope of this Guide and at the discretion of the user.

3.4 The laboratory experimental results described in this document (Appendix 1) were obtained on unpatterned wafers without bumps. The presence of patterns or bumps may induce stresses that will lead to failure at lower force levels than observed in this experiment.

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4 Referenced Standards or Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI G74 — Specification for Tape Frame for 300 mm Wafers

SEMI G87 — Specification for Plastic Tape Frame for 300 mm Wafer

SEMI GXX (SEMI Draft Document 5295) — Specification for Coin-Stack Type Tape Frame Shipping Container for 300 mm Wafer (In Process)

SEMI M31 — Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

4.2 *ISO Standard*[1]

ISO 2248 — Packaging – Complete, filled transport packages – Vertical impact test by dropping

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *3DS-IC* — three dimensional stacked integrated circuit

5.1.2 *TSV* – through silicon via

5.2 *Definitions*

5.2.1 *base, of a wafer shipping box* — the open-top container into which dicing frames carrying wafers are placed, either in cassettes or into integrally molded pockets.

5.2.2 *clamshell wafer shipping container* — a type of stackable wafer shipping container that consists of a base and connected lid that holds a single wafer on a dicing frame.

5.2.3 *coin-stack type shipping container* — a container in which dicing frames carrying wafers are placed horizontally .

5.2.4 *cover, of a wafer shipping box* — the portion of the box which closes at the top of the base.

5.2.5 *cushions* — materials placed between the wafer shipping box and secondary container in order to absorb shock during shipping and to stabilize the wafer shipping box within the secondary container.

5.2.6 *horizontal wafer shipping box* — a wafer shipping box that, when placed upright on its base, holds the wafers such that the front and back surfaces are oriented parallel to the base.

5.2.7 *outer box* — a container part of a shipping box, surrounding the whole objects so as to protect a shipping cassette, except gasket and clamps.

5.2.8 *plastic tape frame* — as described by SEMI G87, a ring-shaped plastic frame to fix a wafer to itself using wafer tape. It is used between the dicing process and the die bonding process, and for the handling and shipping of wafers.

5.2.9 *shipping box* — a protective portable container for a carrier and/or wafer(s) that is used to ship wafers from the wafer suppliers to their customers.

5.2.10 *shipping container* — a carton used to transport wafer boxes; it is typically constructed of corrugated cardboard.

5.2.11 *shipping pack* — a package or shipping container/final container that is of sufficient strength to be used in commerce for packing, storing, and transporting products.

5.2.12 *stackable wafer shipping container* — a wafer shipping box or tray that holds a single wafer on a dicing frame and is designed such that multiple shipping containers may be stacked in small volume.

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[1] International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56 - CH-1211 Geneva 20, Switzerland; central@iso.org; Telephone: +41 22 749 01 11; Fax : +41 22 733 34 30; http://www.iso.org/iso/home.htm

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5.2.13 *tape frame* — the frame that the wafer tape is attached to, as described in SEMI G74 and SEMI G87. The frame supports the tape, which retains the wafer. It is used between the dicing process and the die-bonding process and also used for shipping, handling, and storage of wafers.

5.2.14 *thin silicon wafer* — any silicon wafer which has been fabricated, or mechanically and/or chemically processed, such that its thickness is less than the minimum thickness allowed in a wafer material standard.

5.2.15 *vertical wafer shipping box* — a wafer shipping box that, when stood on its base, holds the wafers such that the front and back surfaces are oriented perpendicular to the base.

5.2.16 *wafer shipping box* — a box that directly holds the wafers. In SEMI M45, this box is specified by SEMI M31.

5.2.17 *wafer shipping tray* — an open-top stackable wafer shipping container where the base of one tray holding a wafer serves as the cover for the next wafer. The cover to the top tray occupied by a wafer is an additional tray which is not holding a wafer.

5.2.18 *wafer tape* — adhesive plastic tape to hold the wafer or cut die.

6 Methods for Shipping Thin Wafers on Dicing Frames

6.1 A number of options are available for shipping thin wafers mounted on dicing tape (Figure 1). These methods are generally based on commercially available methods for shipping full thickness wafers mounted on dicing tape. In the list below the terms “horizontal” and “vertical” refer to the way wafers are oriented in the wafer shipping box when the wafer shipping box is placed in the feet down position. In each case, access to the wafer(s) is from the top of the wafer shipping box.

6.1.1 *Horizontal multi-wafer shipping box* (Figure 2) — a box into which multiple tape frames are stacked. Each tape frame contains exactly one wafer which is attached to the frame using dicing tape. The wafers are prevented from contacting one another using spacers and cushioning material. An example of a horizontal multi-wafer shipping box is the GXX-XX12 (SEMI Draft Document5295), Specification for Coin-Stack Type Tape Frame Shipping Container for 300 mm Wafer

6.1.2 *Horizontal, stackable, single-wafer clamshell* (Figure 3) — a horizontal shipping box with integrated cover tray which holds exactly one wafer mounted on a tape frame using dicing tape. From below, the clamshell contacts the tape directly below the wafer as well the tape directly below tape frame; from above the clamshell contacts the upper surface of the tape frame. Thus, the clamshell holds the tape frame firmly in place during shipment and constrains the wafer from moving relative to the tray without directly contacting the exposed surface of the wafer. Clamshell wafer shipping boxes are typically designed to be stacked during shipment with minimum wasted space.

6.1.3 *Horizontal, stackable, single-wafer tray* (Figure 4) — a tray which holds exactly one wafer mounted on a tape frame using dicing tape. The wafer is held firmly against the bottom of the tray with the tape in tension. Any number of these trays may be stacked with the bottom of the upper tray held at a distance above the wafer. From below, the tray contacts the tape directly below the wafer as well the tape directly below the tape frame; the upper tray contacts only the top surface of the tape frame. This combination holds the tape frame firmly in place during shipment and constrains the wafer from moving relative to the tray without directly contacting the exposed surface of the wafer. The top tray is covered with an additional tray that does not hold a wafer and therefore serves as a cover, thus requiring n + 1 trays to ship n wafers.

6.1.4 *Vertical multi-wafer shipping box* (Figure 5) — a box into which multiple standard tape frames are loaded into guides formed in the shipping box. Each tape frame contains exactly one wafer which is attached to the frame using dicing tape. The guides mechanically prevent the wafers from contact. The mechanical guides may be fabricated in such a way as to hold frames of a specific thickness. Shipping boxes compliant with standard frames are:

6.1.4.1 *Vertical multi-wafer shipping box for G74 compliant metal frame* — thickness of the guides are set to securely hold tape frames of thickness 1.2 mm – 1.5 mm.

6.1.4.2 *Vertical multi-wafer shipping box for G87 compliant plastic frame* — thickness of the guides are set to securely hold tape frames of thickness 2.5 mm.

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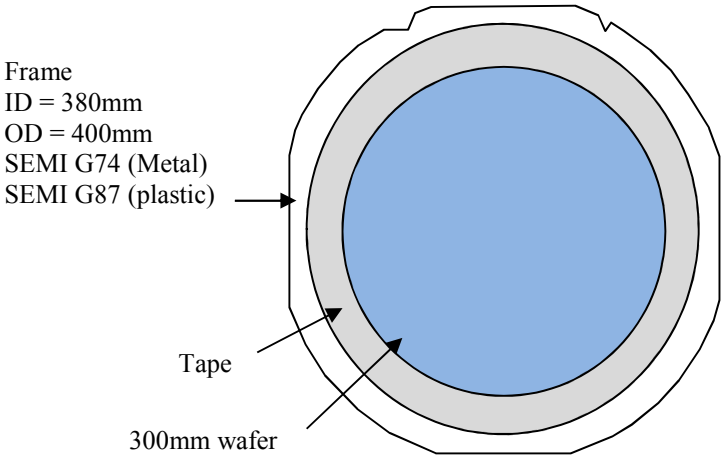

Figure 1
Tape frame with attached 300 mm wafer

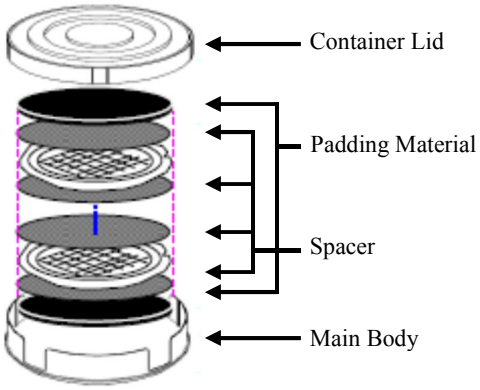

Figure 2
Horizontal Shipping Container (Multi-Wafer)

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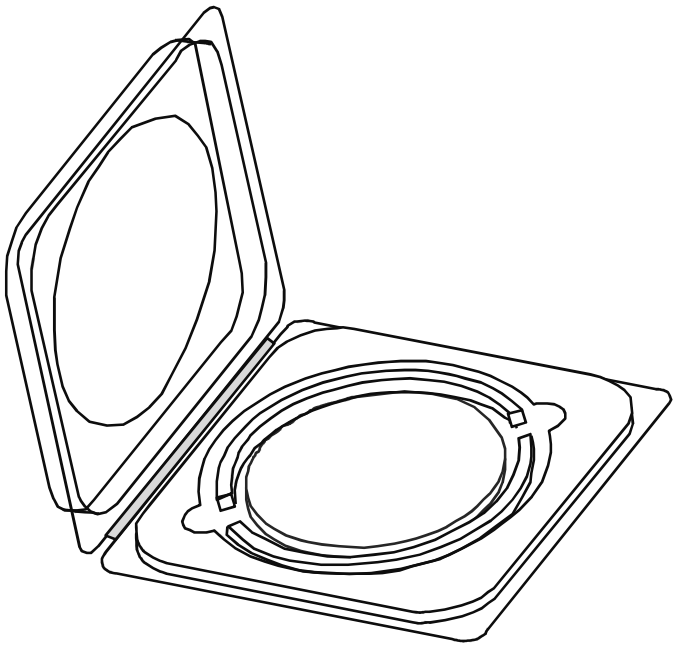

Figure 3
Horizontal Single Wafer Clamshell Container

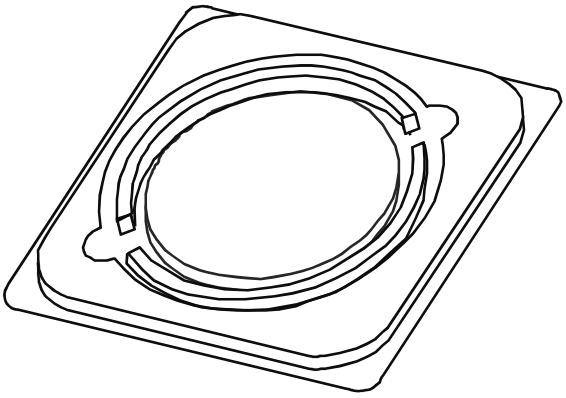

Figure 4
Horizontal Single Wafer Stackable

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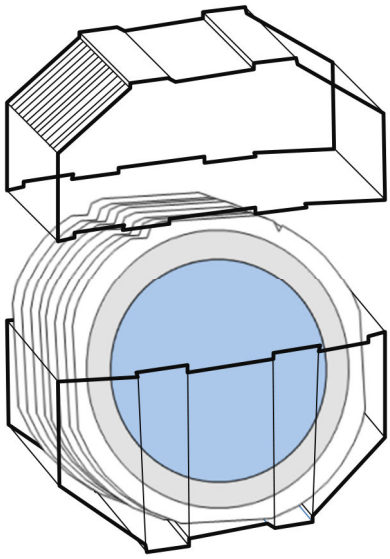

Figure 5
Vertical Shipping Box

7 Acceptance criteria

7.1 Shipping boxes purchased following this guide may be of any of the four types described above or a different type which demonstrates results similar to those shown in Appendix 1. Wafers should be carefully inspected before and after any experimental tests of shipping systems to ensure that any damage is identified.

7.2 Inspection method and criteria

7.3 Wafers will be inspected using visual means before and after shipping

7.3.1 No cracks or no crack growth

7.4 Final inspection performed prior to dicing or bonding

8 Guidelines and Recommendations

8.1 A number of different options for shipping thin wafers mounted on dicing tape were evaluated using wafers of 50 µm and 100 µm thickness. The experimental methods undertaken for the evaluation followed best known methods for wafer grinding (and associated wafer preparatory steps) and used commercially available dicing tapes and dicing frames. Protocols for evaluation included industry standard methodology of shipping drop test, usage of sensors for degree of shock and acceptance criteria, all discussed in this document (Appendix 1).

8.2 Based on the results, all of the options evaluated were adequate in handling both wafer thicknesses. The secondary packaging appears to have a major effect to the integrity of shipping. This is also corroborated by additional data from current practice in product/prototype thin wafer shipping in 3DS-IC manufacturing.

8.3 Ultimately the shipping method needs to be qualified by each user. This document provides a guideline for an experimental procedure that may be used.

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APPENDIX 1
VALIDATION EXPERIMENT AND RESULTS

NOTICE: The material in this appendix is an official part of SEMI [insert designation, without publication date (month-year) code] and was approved by full letter ballot procedures on [insert date of approval by responsible regional standards committee].

A1-1 Description of experiment

A1-1.1 As validation of the methods described in this guide, tests were performed on several different packaging configurations. These packages represent off-the-shelf solutions for shipping full-thickness wafers on dicing tape. The experiments were designed to test the applicability of these solutions for shipping thin wafers. The experiments were performed on wafers thinned to 100 µm and 50 µm and attached to tape on SEMI Standard tape frames. Both types of tape frames were used in the experiment, metal (G74) and plastic (G87). Certain package types are specific for either G74 or G87 frames; these tests were only performed on the appropriate types.

A1-2 Wafer preparation

A1-2.1 A total of 250 prime 300 mm silicon wafers were processed in multiple lots, using several temporary bonding process flows. Half of the wafers were thinned to a final thickness of either 50 µm or 100 µm; the remaining wafers were used as carrier wafers during the thinning process. Available for the experiment after completion of the edge trim and thinning processes were 37 wafers thinned to 50 µm and 46 wafers thinned to 100 µm. All wafers were edge trimmed to a final diameter of between 299 mm and 299.5 mm. Due to differences in portions of the process flows, the 100 µm wafers can further be split into 37 wafers with poor edge quality and 9 wafers with good edge quality.

A1-2.2 The process flows conclude with thinned wafers attached to a tape frame using UV curable dicing tape as shown in Figure 1 of the Guide These tape frames are either metal, conforming to SEMI G74, or plastic, conforming to SEMI G87.

A1-2.3 The thin wafers were inspected for cracks and edge defects; cracked wafers were eliminated from the experiment.

A1-2.4 The tape frames, with the thin wafers attached, were packaged into shipping boxes. When provided, the shipping box manufacturers' recommendations for box choice were used.

A1-2.5 Single trigger shock sensors with trigger values between 10g and 75g were attached to the outer surfaces of the primary shipping boxes at an orientation corresponding to the drop attitude (§ A1-2.7). These sensors are triggered if exposed to a force whose component in a specific axis, or axes, is greater than a threshold value. When triggered, the liquid inside of the sensor changes color, typically to a bright red. The sensor may come as a tube or in an adhesive package. A diagram showing the tubes and the sensitivity orientation is shown in Figure A1-1.

A1-2.6 Shipping boxes were packaged into secondary packaging. For cases where the shipping box manufacturer provides or recommends secondary packaging, their secondary packaging was used; otherwise, secondary packaging was chosen based on best practice.

A1-2.7 *Test attitude* — refers to the orientation of the package on impact and the drop test on the shipping package may be performed such that the impact is to a face (six total), an edge (twelve total), or a corner (eight total). Due to symmetry considerations, a full experiment can be performed with less than a complete set of 26 drop tests. The actual number of required drops to cover the various attitudes is dependent on the shipping box and secondary packaging configuration.

A1-2.8 Appendix 2 includes a description of finite element modeling performed to support this experiment.

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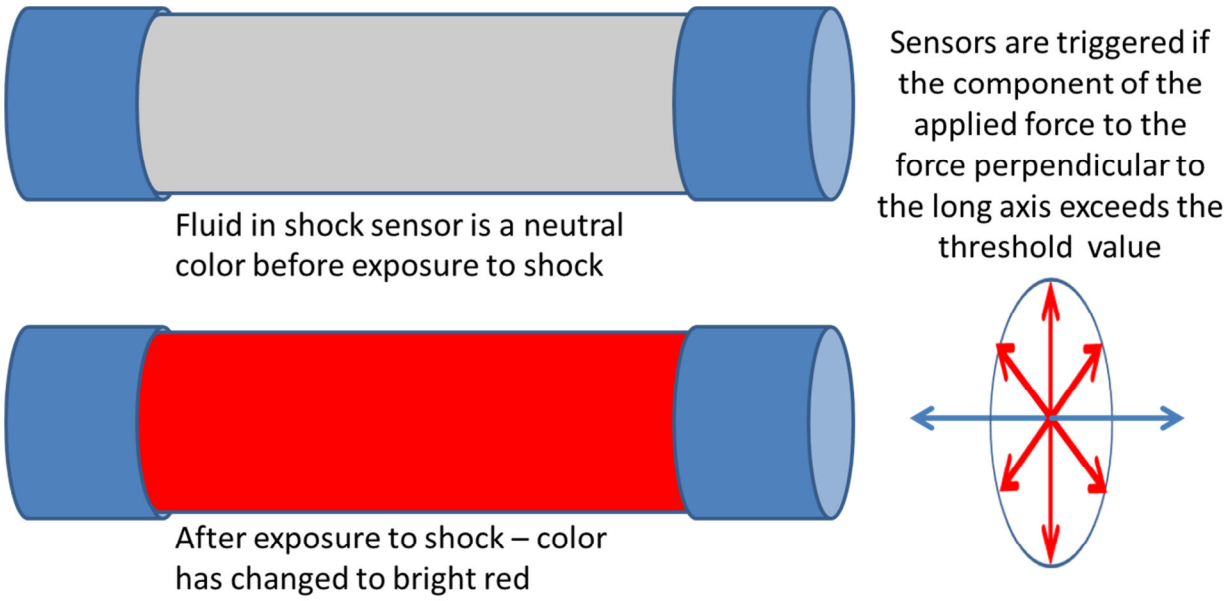

Figure A1-1
Details of the active component of a typical shock sensor

A1-3 Experimental results

A1-3.1 *Summary* — The drop tests were performed on all packaging configurations in two sessions based on thin wafer availability; the first session used only the 37 100 µm thick wafers with poor edge quality; the second session included both types of 100 µm wafers as well as 50 µm wafers co-packaged. The second set of tests included the 100 µm thick wafers from Lot 1 and Lot 2b side-by-side to see if the edge quality affected the results. None of the shipping containers failed in any drop, e.g., in no case did all wafers under test break.

A1-3.2 Secondary packaging appeared to play a significant role in the results. That is, the wafers are held firmly in place by each configuration, with the primary packaging attenuating minimal part of the impact force. In addition, the forces delivered to the secondary packaging from the higher, 1200 mm drops, caused visible damage to the secondary packaging in some cases.

A1-3.3 *800 mm drop test results* — an 800 mm drop roughly corresponds to an unpadded drop with a shock of 100 g.

A1-3.3.1 The 800 mm drops yielded no breakage to the good edge quality wafers, that is, to neither the 50 µm nor he 100 µm thick wafers. There were random instances of the poor edge quality wafers breaking in 800 mm drops, but this did not correlate to observed breakage in the 1200 mm drops.

A1-3.4 *1200 mm drop test results* — a 1200 mm drop roughly corresponds to an unpadded drop with a shock of 150 g.

A1-3.4.1 The 1200 mm drop tests also yielded breakage of a small number of wafers; the breakage occurred only to 50 µm wafers or 100 µm wafers with poor edge quality. These breaks did not correspond to any particular attitude, frame type, or package. In cases where the breakage occurred to wafers packaged in a multi-wafer shipping box, in no case did all wafers break.

A1-3.5 *Shock sensor* — the placement of the shock sensors on the shipping box should identify the maximum force that the wafers are exposed to upon impact. In practice, the sensors as-used only provided semi-quantitative information on the force of impact. Part of this may be due to the difficulty in placing the sensors so that their long edges were perpendicular to the direction of impact.

A1-3.5.1 *Shock sensors for 800 mm drop* — the sensors recorded maximum impacts of either 37 g or 50 g, depending, on attitude.

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A1-3.5.2 *Shock sensors for 1200 mm drop* — the sensors typically recorded maximum impacts of either 50 g or 75 g, depending on attitude.

A1-3.5.3 *Secondary packaging* — the secondary packaging appeared to play a role in system performance, with the impact sensors recording lower impacts from packages with better secondary packaging.

A1-3.5.4 This appears to be a key performance indicator.

A1-4 Field observations on shipped thinned wafers

A1-4.1 In the past two years, some of leading semiconductor companies have shipped more than one thousand wafers for evaluations as well as for product assembly without any major issues. It appears that with adequate secondary packaging any of shipping solutions discussed in §6 of the Guide can be used.

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APPENDIX 2
FINITE ELEMENT MODELING OF THIN SILICON WAFER MOUNTED ON TAPE FRAME

NOTICE: The material in this Appendix is an official part of SEMI [designation number] and was approved by full letter ballot procedures on [A&R approval date].

A2-1 Fracture Toughness of Silicon

A2-1.1 The fragility of silicon wafers is well known, with breakage concerns leading to wafer thicknesses of 10 mil2[2] (279 μm) for 2" (50.8 mm) diameter wafers to 925 μm for 450 mm wafers. 3D stacking reverses this trend, requiring thin wafers – less than 100 μm – to allow fabrication of TSVs. Further, 3D process flows are projected to involve shipping thinned wafers from fabrication site to a site where the wafers will be stacked. Common shipping methods for standard wafers have been established, e.g., FOSBs (SEMI M31) But the well-known fragility of thin wafers is an obstacle to this prospect, because thin wafers can be damaged during shipping, even when the shipping method used would be adequate for full-thickness wafers. The failure mode for silicon wafers under shipping conditions is brittle fracture, as discussed by Cook[3]. Conditions for brittle fracture can be described in terms of three quantities: the applied stress; the relevant crack size; and the fracture toughness of the material.

A2-1.2 Cook tabulates the fracture toughness of silicon for the various important crystallographic directions. But the effective crack size for silicon wafers must be determined on a case-by-case basis, although Cook gave some guidelines. In the work cited, Cook stated: "However, under normal handling circumstances, over large areas comparable to that of the wafer, there is likely to be a defect of order 50 μm, about 1/10 of the wafer thickness, leading to strengths of order 100 MPa. Treating the strength of polished Si surface as an intrinsic parameter…: A design strength of 130 MPa for a (001) wafer seems appropriate in this regard." Cook's paper refers to full-thickness wafers. The value of an appropriate design strength for well-polished thin wafers, or even the existence of such a parameter, has yet to be determined by experiment; it is to be expected that the value of this design strength can decrease significantly if the wafers are not in a well-polished condition.

A2-1.3 The benefit of having a value for this design strength would be that wafer shipping materials, known as "wafer shipping boxes" and "secondary packaging," could be designed and evaluated by mechanics analysis, by calculating the stress in the wafer under shipping conditions. In order to begin accumulating data about the stress values in wafers under shipping conditions, an approximate mechanics analysis of the experiments noted above was performed.

A2-2 Shipping Configurations

A2-2.1 The key shipping condition considered was a drop of a package containing one or more wafers, each carried on a dicing frame (tape frame). This parallels the experiment described in Appendix 1 of this Guide. The strategy adopted was to treat the wafer-tape-frame assembly separately from the secondary packaging. The wafer-tape-frame assembly was treated by finite element analysis (FEA), while the effect of the secondary packaging was included in the analysis as a "stopping distance". The "stopping distance" is the distance that the wafer frame travels during its deceleration from free fall to stationary. This stopping distance is provided by the resiliency of the secondary packaging materials, including any cushioning materials if present. With an assumed stopping distance and the assumption of "ideal cushioning", which means that the peak negative acceleration (or deceleration) of the frame is taken as the minimum possible value needed to bring the falling frame to a stop, the profile of acceleration versus time applied to the wafer frame can be evaluated. This acceleration profile can be input into a dynamic finite element analysis (DFEA); from this analysis, the stress at any point on the wafer can be calculated as a function of time.

A2-2.2 For conditions of the experiments, specifically, drops of 800 and 1200 mm, stress values lower than Cook's value of 130 MPa were calculated. Yet, in the first set of experiments, wafers broke in the wafer shipping boxes with the least cushioning. The impact detectors included in the packages supported the acceleration values in the calculation. A likely cause of the breaks soon came to light: the wafers used had damage at the edges. This damage

[2] Standard dimension for 2" and 3" diameter wafers follow U.S. customary units; standard dimensions for 100 mm and larger diameter wafers follow SI units.

[3] R. F. Cook, Strength and sharp contact fracture of silicon, Journal of Materials Science. 2006, 41, 841-872.

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formed stress concentrations, and perhaps even cracks, which caused the wafers to break. The second set of experiments, conducted using wafers with undamaged edges, gave different results. In these experiments, wafers only broke when the primary packaging was damaged.

A2-2.3 *Z-direction drops*

A2-2.3.1 The stresses calculated for the centers of the wafers in the "z-direction drops" were higher than those at the edges of the wafers, and were of the order of two-thirds of Cook's 'design strength' of 130 MPa (see Figure A1-1). No breaks were seen in the centers of the wafers.

A2-2.3.2 Figure A1-1 also shows asymmetries in the displacements, even in what should be a drop orthogonal to the plane of the wafer. These asymmetries appear to be associated with the two notches and four flats (see Figure 1) which appear on tape frames which conform to SEMI G74 or G87.

A2-2.4 It is concluded from the above that mechanics analysis can provide additional insight, but cannot replace, experiments on the efficacy of particular shipping containers in preventing wafer damage during shipping.

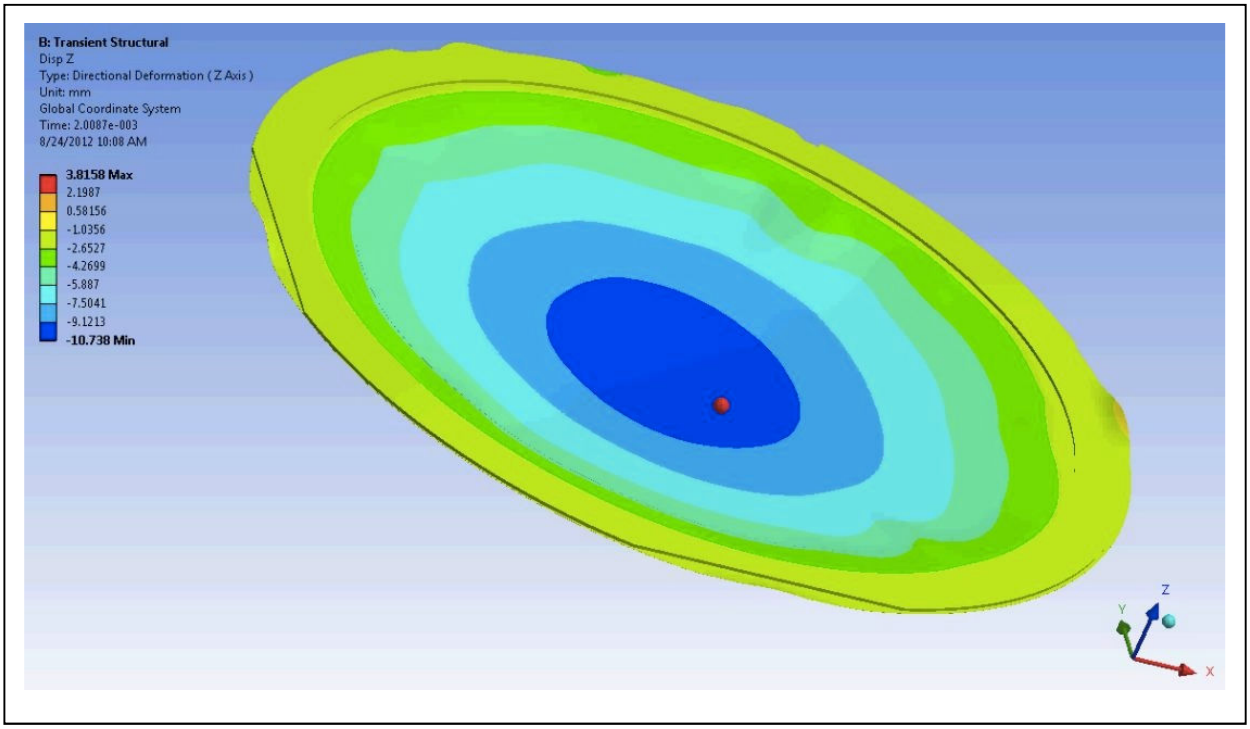

Figure A2-1

Single time step from a model showing displacement from the plane of a 300 mm wafer

NOTE: The wafer in this simulation was subject to a "z-direction drop" and the stress applied to different regions of the wafer is a function of the displacement. This shows that the maximum stress is near the center of the wafer, rather than the edges. Also note the asymmetry of the displacements; this is apparently due to the presence of notches and/or flats on the tape frame.

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